Mercury KX1 FPGA Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury KX1 FPGA module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury KX1 FPGA module.

Summary

This document first gives an overview of the Mercury KX1 FPGA module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-KX1	Mercury KX1 FPGA Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-411-002	07	16.02.2021

Approval Information	Name	Position	Date
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Document History

Version	Date	Author	Comment
07	16.02.2021	DIUN	Cleaned-up product variants, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
06	25.07.2019	DIUN	Added information on voltage monitoring, power supplies, heat sink, updated DDR memory types and EEPROM map description, other style updates
05	21.08.2018	DIUN	Minor corrections and style updates
04	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
03	27.12.2016	DIUN	Added tool support information
02	02.08.2016	DIUN	Version 02, added information on MGTs
01	05.07.2016	DIUN	Version 01

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mercury KX1 FPGA module combines the Xilinx Kintex-7® All Programmable FPGA device with fast DDR3 SDRAM, USB 3.0 controller and PHY, dual Gigabit Ethernet, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mercury KX1 FPGA module, in contrast to building a custom FPGA hardware, significantly simplifies system design and thus shortens time to market and decreases the development effort of your product.

Together with Mercury base boards, the Mercury KX1 FPGA module allows the user to quickly build a system prototype and start with application development.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mercury KX1 FPGA module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury KX1 FPGA module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury KX1 FPGA module.

1.1.5 Safety Recommendations and Warnings

Mercury modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury KX1 FPGA module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

It is possible to mount the Mercury KX1 FPGA module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury KX1 FPGA module.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

Warning!

Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

Always check that the mounting holes on the Mercury+ PE1 base board are aligned with the mounting holes of the Mercury KX1 FPGA module. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury KX1 FPGA module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Kintex-7 28 nm FPGA XC7K160T/XC7K325T, FFG676/FBG676 package
- 178 user I/Os up to 3.3 V
  - 158 FPGA I/Os (single-ended, differential or analog)
  - 20 MGT signals (clock and data)
- *FBG package devices*: 4 MGTs @ 6.6 Gbit/sec and 2 reference input clock differential pairs
- *FFG package devices*: 4 MGTs @ 10.3125 Gbit/sec and 2 reference input clock differential pairs
- PCIe Gen2 ×4 (Xilinx integrated PCIe block)
- Up to 2 GB + 512 MB DDR3 SDRAM
- 64 MB quad SPI flash
- Cypress EZ-USB FX3 USB 3.0 device controller
- Dual Gigabit Ethernet
- Real-time clock
- High-power 16 A core power supply
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury KX1 FPGA module
- Mercury KX1 FPGA module documentation, available via download:
  - Mercury KX1 FPGA Module User Manual (this document)
  - Mercury KX1 FPGA Module Reference Design [2]
  - Mercury KX1 FPGA Module IO Net Length Excel Sheet [3]
  - Mercury KX1 FPGA Module FPGA Pinout Excel Sheet [4]
  - Mercury KX1 FPGA Module User Schematics (PDF) [5]
  - Mercury KX1 FPGA Module Known Issues and Changes [6]
  - Mercury KX1 FPGA Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mercury KX1 FPGA Module 3D Model (PDF) [8]
  - Mercury KX1 FPGA Module STEP 3D Model [9]
  - Mercury Mars Module Pin Connection Guidelines [10]
  - Mercury Master Pinout [11]
  - Mercury Heatsink Application Note [15]

1.4 Accessories

1.4.1 Reference Design

The Mercury KX1 FPGA module reference design features an example configuration for the Kintex-7 FPGA device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.4.2 Mercury+ PE1 Base Board

- 168-pin Hirose FX10 module connectors (PE1-200: 2 connectors; PE1-300/400: 3 connectors)
- System controller
- Power control
- System monitor (PE1-300/400)
- Current sense (PE1-300/400)
- Low-jitter clock generator (PE1-300/400)
- microSD card holder
- User EEPROM
- eMMC managed NAND flash (PE1-300/400)
- PCIe $\times 4$ interface
- USB 3.0 device connector
- USB 2.0 host connector (PE1-200: 1 connector; PE1-300/400: 4 connectors)
- Micro USB 2.0 device (UART, SPI, I2C, JTAG) connector
- 2 $\times$ RJ45 Gigabit Ethernet connectors
- mPCIe/mSATA card holder (USB only) (PE1-300/400)
- SIM card holder (optional, PE1-300/400 only)
- SMA clock and data in/out (optional, PE1-300/400 only)
- 1 $\times$ FMC LPC connector (PE1-200)
- 1 $\times$ FMC HPC connector (PE1-300)
- 2 $\times$ FMC LPC connector (PE1-400)
- 2 $\times$ 40-pin Anios pin header
- 3 $\times$ 12-pin IO headers
- 5 to 15 V DC supply voltage
- USB bus power (with restrictions)

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

1.4.3 Mercury+ ST1 Base Board

- 168-pin Hirose FX10 module connectors (3 connectors)
- 2 × MIPI D-PHY connectors: CSI and CSI/DSI (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- SFP+ connector
- Low-jitter clock generator
- USB 3.0 device connector
- USB 3.0 host connector
- FTDI USB 2.0 device controller with micro USB device connector (UART, SPI, I2C, JTAG)
- 2 × RJ45 Gigabit Ethernet connectors
- 1 × FMC HPC connector (note: not all pins are available)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- microSD card holder
- 5 to 15 V DC supply voltage
- Form factor: 100 × 120 mm

Please note that the available features depend on the equipped Mercury module type.

1.5 Xilinx Tool Support

The FPGA devices equipped on the Mercury KX1 FPGA module are supported by the Vivado HL WebPACK Edition or by the Vivado HL Design Edition software, depending on the device's density. Table 1 presents the correspondence between devices and tools. Please contact Xilinx for further information.

Module	Xilinx Tool Support	Costs
ME-KX1-160	Vivado HL WebPACK Edition	Free of charge
ME-KX1-325	Vivado HL Design Edition	Paid license required

Table 1: Xilinx Tool Support

2 Module Description

2.1 Block Diagram

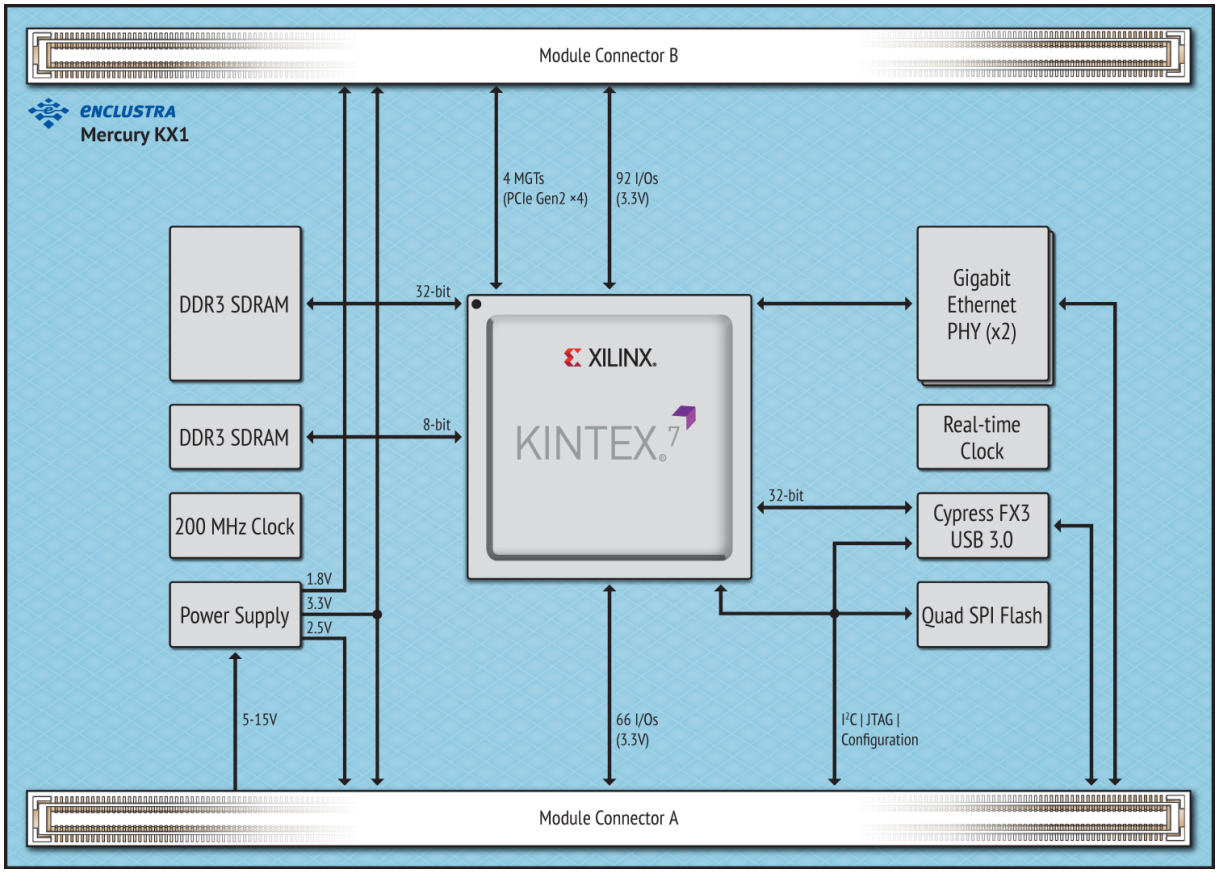

Figure 1: Hardware Block Diagram

The main component of the Mercury KX1 FPGA module is the Xilinx Kintex-7 FPGA device. Most of its I/O pins are connected to the Mercury module connectors, making 158 regular user I/Os available to the user. Further, four multi-gigabit transceivers with support for PCIe Gen2 ×4 are available on the module connector.

The FPGA device can be configured with a bitstream residing in the on-board QSPI flash, via Cypress FX3 USB 3.0 controller fitted on the module, via an external microcontroller or via the JTAG interface connected to Mercury module connector.

The memory subsystem is built from a 64 MB QSPI flash and up to 2 GB + 512 MB DDR3 SDRAM in the standard configuration.

Further, the module is equipped with two Gigabit Ethernet PHYs, making it ideal for communication applications.

A Cypress FX3 USB 3.0 controller is fitted on the module to easily implement a communication link to a host PC.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 100 MHz crystal oscillator and on a 200 MHz LVDS oscillator.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Four LEDs are connected to the FPGA pins for status signaling. Another LED is connected to the Cypress FX3 USB 3.0 controller user pin for the same purpose.

2.2 Module Configuration and Product Codes

Table 2 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	FPGA	DDR3/DDR3L SDRAM	USB 3.0	Temperature Range
ME-KX1-160-1C-D10	XC7K160T-1FBG676C	1024 + 256 MB	✓	0 to +70° C
ME-KX1-325-2I-D11-P	XC7K325T-2FFG676I	2048 + 512 MB	✓	-40 to +85° C

Table 2: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

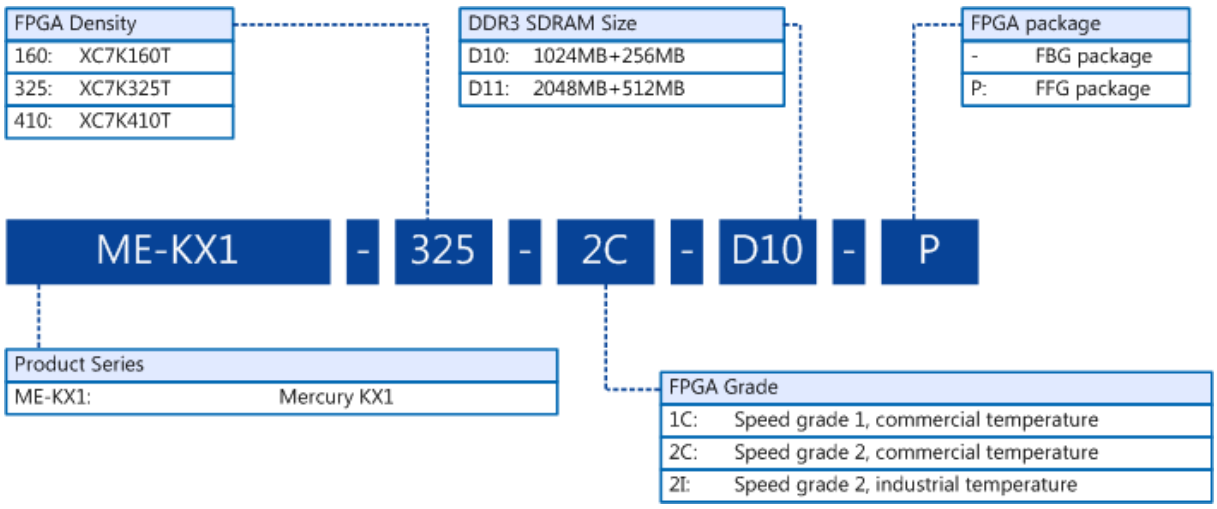

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

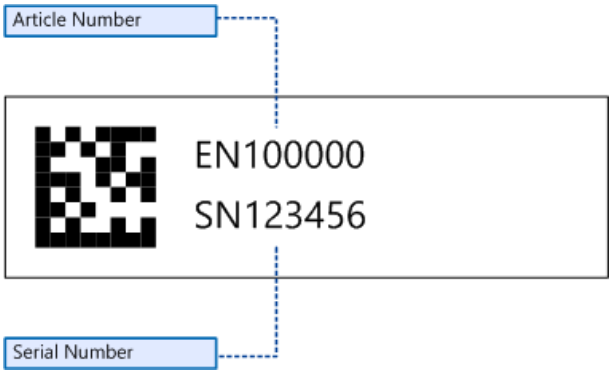

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 3. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury KX1 FPGA Module Known Issues and Changes document [6].

Article Number	Article Code
EN100029	ME-KX1-160-1C-D10-R2
EN100004	ME-KX1-325-2I-D11-P-R2
EN100089	ME-KX1-325-1C-D10-R2
EN100590	ME-KX1-410-2I-D11-P-R2
EN100871	ME-KX1-410-2C-D11-P-R2
EN101015	ME-KX1-160-1C-D10-R3
EN101421	ME-KX1-160-1C-D10-R3
EN101017	ME-KX1-325-2I-D11-P-R3
EN101515	ME-KX1-325-2C-D10-P-R3
EN101018	ME-KX1-410-2I-D11-P-R3
EN101422	ME-KX1-325-1C-D10-R4
EN101016	ME-KX1-325-1C-D10-R4
EN101519	ME-KX1-160-1C-D10-R4.1
EN101520	ME-KX1-325-2I-D11-P-R4.1
EN101424	ME-KX1-410-2I-D11-P-R4.1
EN101816	ME-KX1-160-1C-D10-R5
EN101921	ME-KX1-325-2C-D10-P-R5
EN101818	ME-KX1-325-2I-D11-P-R5
EN101819	ME-KX1-410-2I-D11-P-R5

Table 3: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

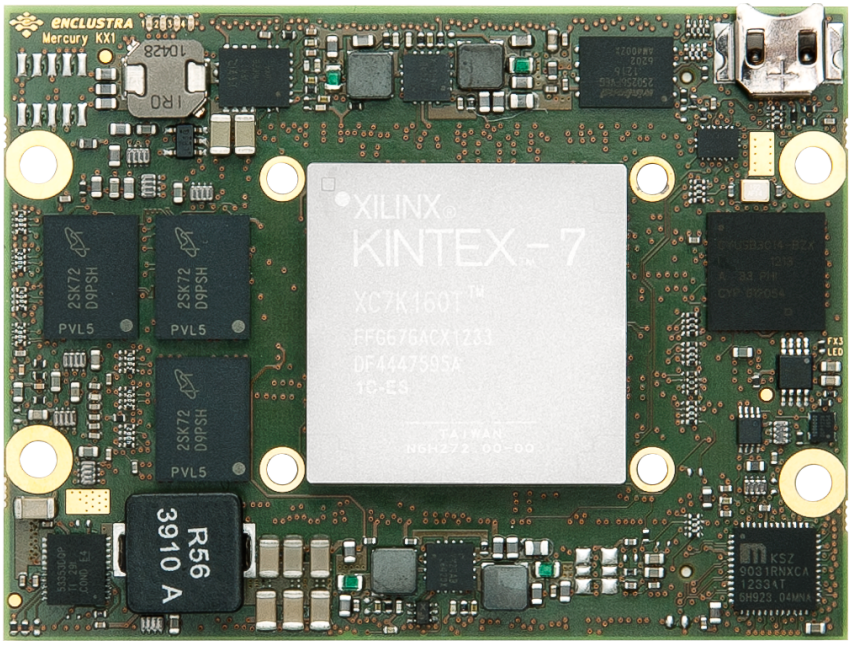

Figure 4: Module Top View

2.4.2 Bottom View

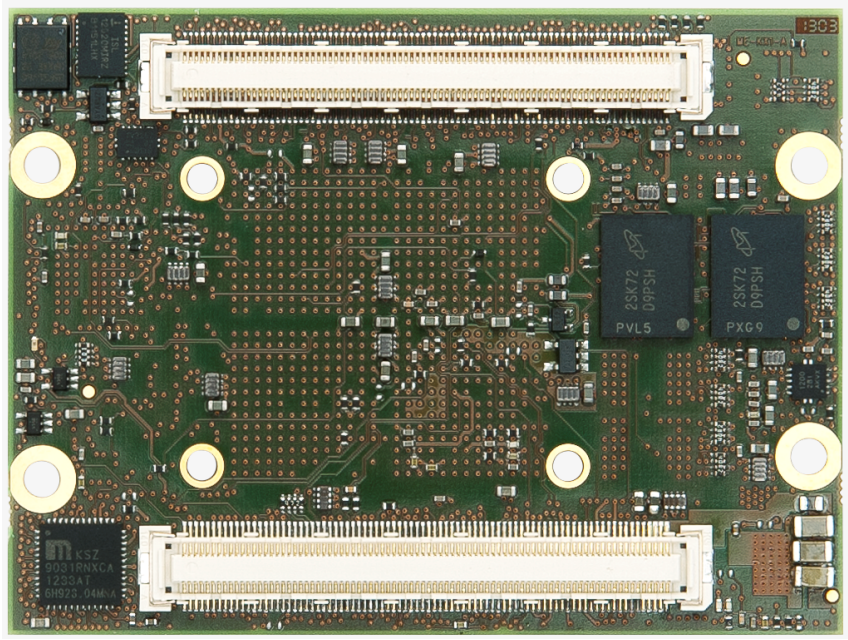

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

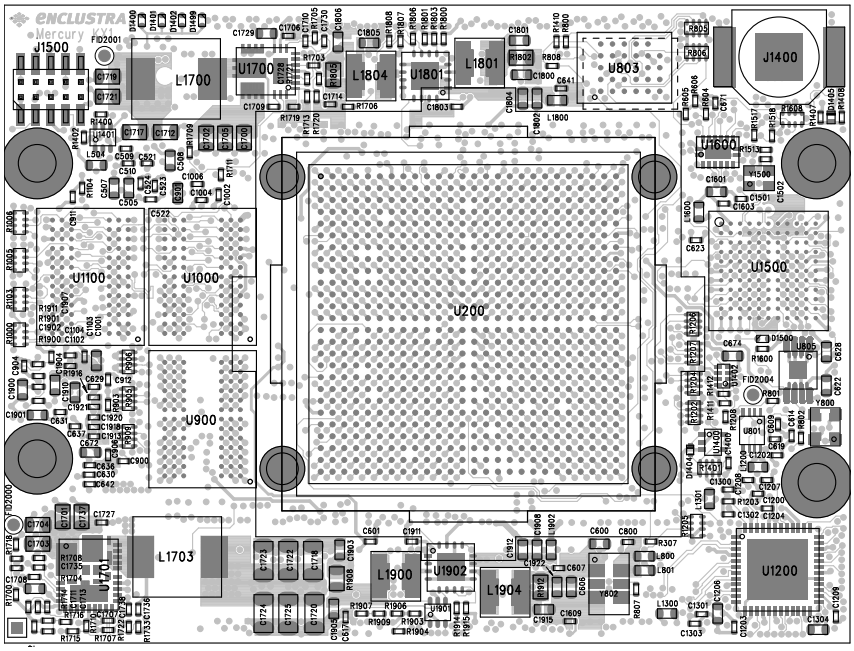

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

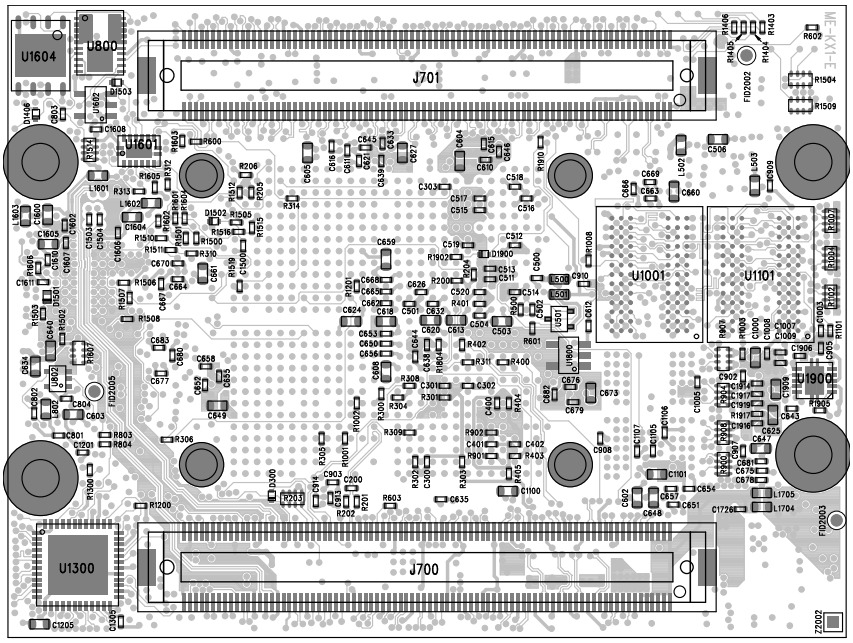

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height on the base board under the module is dependent on the connector type. Please refer to the Hirose FX10 series product website for detailed connector information [12].
The two connectors are called A (J700) and B (J701).

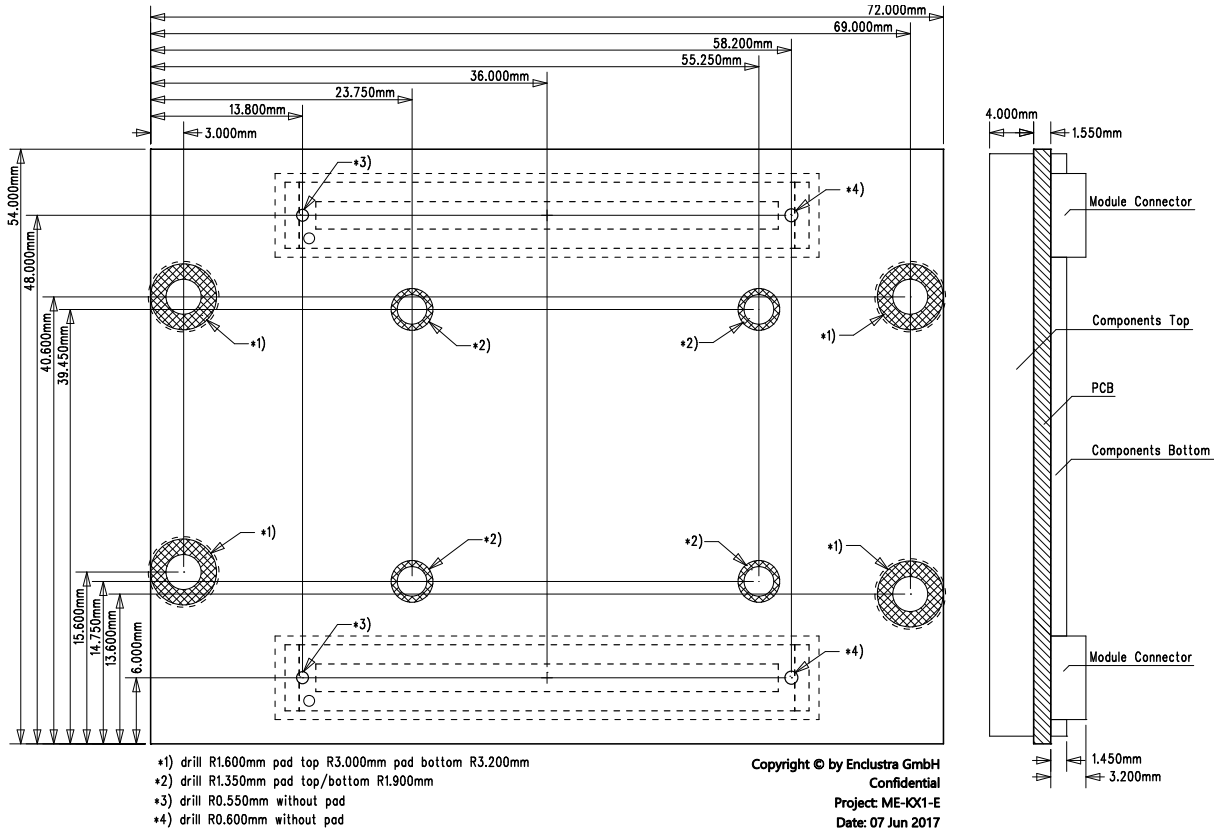

Figure 8: Module Footprint - Top View

Warning!

It is possible to mount the Mercury KX1 FPGA module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury KX1 FPGA module.

2.7 Mechanical Data

Table 4 describes the mechanical characteristics of the Mercury KX1 FPGA module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	72 × 54 mm
Component height top	4.0 mm
Component height bottom	1.45 mm
Weight	32 g

Table 4: Mechanical Data

2.8 Module Connector

Two Hirose FX10 168-pin 0.5 mm pitch headers with a total of 336 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 5. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 5: Module Connector Types

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J700-1 to J700-168
- Connector B: from J701-1 to J701-168

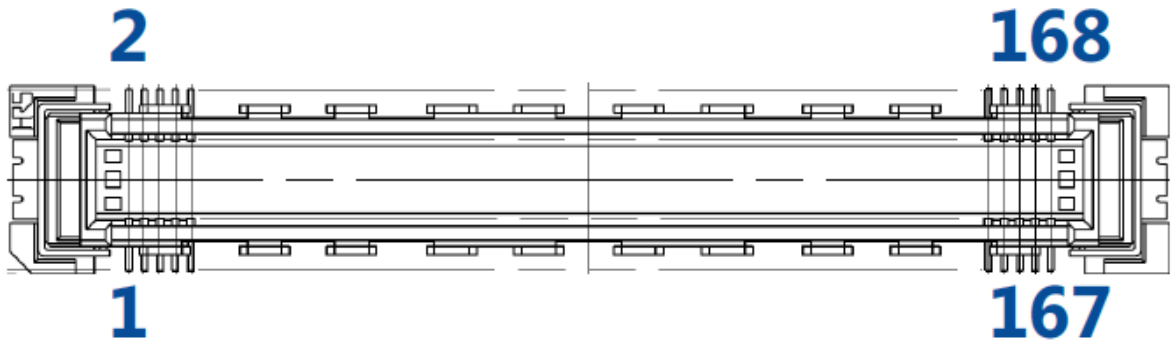

Figure 9: Pin Numbering for the Module Connector

Warning!

Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.

2.9 User I/O

2.9.1 Pinout

Information on the Mercury KX1 FPGA module pinout can be found in the Enclustra Mercury Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury KX1 FPGA module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR>_<SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>

For example, IO_B15_L12_MRCC_AD5_E17_N is located on pin E17 of I/O bank 15, pair 12, it is an MRCC (Multi-Region Clock Capable) pin and also an XADC auxiliary analog input capable pin, and it has negative polarity, when used in a differential pair.

The multi-region clock capable pins are marked with "MRCC", while the single region clock capable pins are marked with "SRCC" in the signal name. For details on their function and usage, please refer to the Xilinx documentation.

Table 6 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_B12_<...>	48	24	In/Out	In/Out	12
IO_B13<...>	18	9	In/Out	In/Out	13
IO_B15<...>	44	22	In/Out	In/Out	15
IO_B16<...>	48	24	In/Out	In/Out	16
Total	**158**	**79**	-	-	-

Table 6: User I/Os

Please note that for the 7 Series FPGAs there are restrictions on the VCCO voltage when using LVDS I/Os; refer to Xilinx AR# 43989 for details.

2.9.2 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the FPGA device to the module connector is available in Mercury KX1 FPGA Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mercury KX1 FPGA module. Please use the information provided in the Mercury KX1 FPGA Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

2.9.3 I/O Banks

Table 7 describes the main attributes of the FPGA I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
MGT Bank 115	Not connected	1.2 V	-
MGT Bank 116	Module connector	1.2 V	-
Bank 0	Configuration (JTAG, QSPI)	User selectable VCC_CFG_B13	-
Bank 12	Module connector	User selectable VCC_IO_B12	IO_B12_L6_VREF_W21_N IO_B12_L19_VREF_AE21_N
Bank 13	Module connector, I2C, Ethernet PHYs	User selectable VCC_CFG_B13	-

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
Bank 14	QSPI flash, FX3 USB 3.0 controller	User selectable VCC_CFG_B13	-
Bank 15	Module connector, LEDs	User selectable VCC_IO_B15	IO_B15_L6_VREF_D16_N IO_B15_L19_A21_VREF_J20_N
Bank 16	Module connector	User selectable VCC_IO_B16	IO_B16_L6_VREF_H11_N IO_B16_L19_VREF_C13_N
Bank 32	DDR3B	User selectable[1] VCC_DDR3L	-
Bank 33	DDR3B	User selectable[1] VCC_DDR3L	0.5 × VCC_DDR3L
Bank 34	DDR3A	User selectable[1] VCC_DDR3L	0.5 × VCC_DDR3L

Table 7: I/O Banks

2.9.4 VREF Usage

I/O standards referenced using VREF can be used on the Mercury module connector. The reference voltage has to be applied to all VREF pins of the respective I/O banks. If a bank is configured to use an I/O standard that does not need a reference voltage, the VREF pins of this bank on the module connector are available as user I/O pins.

The VREF pins are listed in the Mercury Master Pinout Excel Sheet [11].

Warning!

Use only VREF voltages compliant with the equipped FPGA device; any other voltages may damage the equipped FPGA device, as well as other devices on the Mercury KX1 FPGA module.

Do not leave a VREF pin floating when the used I/O standard requires a reference voltage, as this may damage the equipped FPGA device, as well as other devices on the Mercury KX1 FPGA module.

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x] or VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

[1]The DDR3 SDRAM supports voltages of 1.5 or 1.35 V. Please refer to Section 2.15 for details.

Signal Name	FPGA Pins	Supported Voltages	Connector A Pins	Connector B Pins
VCC_IO_B12	VCCO_12	1.0 V - 3.3 V ±5%	38, 41	-
VCC_CFG_B13	VCCO_0 VCCO_13 VCCO_14	1.8 V[2], 2.5 V - 3.3 V ±5%	74, 77	-
VCC_IO_B15	VCCO_15	1.0 V - 3.3 V ±5%	-	140, 143
VCC_IO_B16	VCCO_16	1.0 V - 3.3 V ±5%	-	64, 67, 88, 95

Table 8: VCC_IO Pins

Note that the CFGBVS_0 pin is set automatically to GND (if VCC_CFG_B13 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_B13 is 2.5 V or 3.3 V).

Warning!

Use only VCC_IO voltages compliant with the equipped FPGA device; any other voltages may damage the equipped FPGA device, as well as other devices on the Mercury KX1 FPGA module.

Do not leave a VCC_IO pin floating, as this may damage the equipped FPGA device, as well as other devices on the Mercury KX1 FPGA module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 10 illustrates the VCC_IO power requirements.

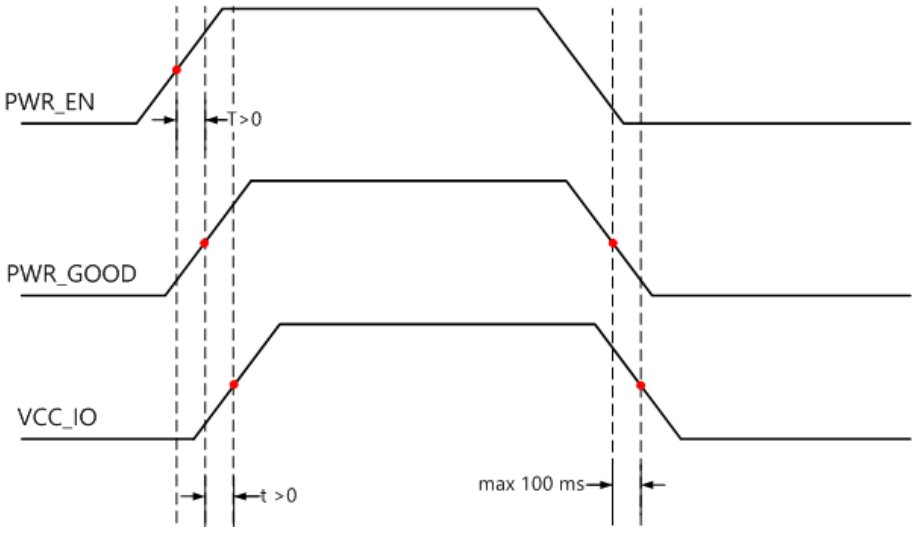

Figure 10: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

[2] 1.8 V support is only available for modules of revision 3 and newer.

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mercury KX1 FPGA module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the FPGA device's internal termination resistors.

Internal differential termination is available only for certain VCCO voltages; please refer to Xilinx AR# 43989 for details.

Single-Ended Outputs

There are no series termination resistors on the Mercury KX1 FPGA module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 Analog Inputs

The Kintex-7 FPGA devices provide a dual 12-bit ADC. The auxiliary analog inputs of the FPGA device are connected to the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name.

The two dedicated ADC pins VP and VN are available on the module connector on pins A-110 and A-112 (FPGA_V_P/N). The ADC can also be used for internal voltage and temperature monitoring. For detailed information, refer to the Xilinx 7 Series XADC User Guide [16].

The ADC lines are always used differentially; for single-ended applications, the *_N line must be connected to GND.

Table 9 presents the ADC Parameters.

Parameter	Value
VCC_ADC	1.8 V
GND_ADC	0 V (connected to GND via ferrite)
VREF_ADC	1.25 V
ADC Range	0-1 V
Sampling Rate per ADC	1 MSPS
Total number of channels	12 (1 dedicated channel, 11 auxiliary inputs)

Table 9: ADC Parameters

2.10 Multi-Gigabit Transceiver (MGT)

Four Multi-Gigabit transceivers and two reference input clock differential pairs are routed directly to the module connector B.

Table 10 lists the available speeds for the MGT lines on the FPGA device. Refer to Section 2.2 for details on the module configurations and equipped FPGA devices.

MGT Speed	FPGA Device
6.6 Gbit/sec	FPGA devices of speedgrade -1 or in FBG package
10.3125 Gbit/sec	FPGA devices of speedgrade -2 in FFG package

Table 10: MGT Switching Characteristics on the Mercury KX1 FPGA module

Warning!

The maximum data rate on the MGT lines on the Mercury KX1 FPGA module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.

Warning!

No AC coupling capacitors are placed on the Mercury KX1 FPGA module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.

2.11 Power

2.11.1 Power Generation Overview

The Mercury KX1 FPGA module uses a 5 - 15 V DC power input for generating the on-board supply voltages (1.0 V, 1.2 V, 1.35 V/1.5 V, 1.8 V, 2.0 V, 2.5 V and 3.3 V). Some of these voltages (1.8 V, 2.5 V, 3.3 V) are accessible on the module connector.

Table 11 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V0	1.0 V	20 A	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	2 A	VCC_3V3	Yes	Yes
VCC_DDR3	1.35 V/1.5 V	2 A	VCC_3V3	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_3V3	Yes	Yes
VCC_2V0[3]	2.0 V	0.15 A	VCC_2V5	Yes	No
VCC_2V5	2.5 V	2 A	VCC_3V3	Yes	Yes
VCC_3V3	3.3 V	9 A	VCC_MOD	No	Yes

Table 11: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

[3] The 2.0 V LDO is equipped only for FPGA devices in FFG packages.

2.11.2 Power Enable/Power Good

The Mercury KX1 FPGA module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.0 V, 1.2 V, 1.35/1.5 V, 1.8 V, and 2.5 V. The 3.3 V supply is always active.

The PWR_EN input is pulled to VCC_3V3 on the Mercury KX1 FPGA module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury KX1 FPGA module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.11.1.

The PWR_GOOD signal is also connected to an FPGA pin via a 47 kΩ resistor.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 12: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mercury KX1 FPGA module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins (for example by connecting VCC_3V3 to VCC_IO directly) when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 10.

2.11.3 Voltage Supply Inputs

Table 13 describes the power supply inputs on the Mercury KX1 FPGA module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V ±5%	Supply for the 1.0 V and 3.3 V voltage regulators. All other supplies are generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.0 - 3.6 V	Battery for the RTC and FPGA encryption key storage

Table 13: Voltage Supply Inputs

2.11.4 Voltage Supply Outputs

Table 14 presents the supply voltages generated on the Mercury KX1 FPGA module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[4]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155	3.3 V ±5%	3 A (and max 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89	2.5 V ±5%	1.2 A	Controlled by PWR_EN
VCC_1V8	B-52, 76, 108, 128	1.8 V ±5%	1.2 A	Controlled by PWR_EN

Table 14: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury KX1 FPGA module.

2.11.5 Power Consumption

Please note that the power consumption of any FPGA device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

2.11.6 Heat Dissipation

High performance devices like the Xilinx Kintex-7 FPGA need cooling in most applications; always make sure the FPGA is adequately cooled.

Table 15 lists the heat sink and thermal pad part numbers that are compatible with the Mercury KX1 FPGA module.

Product Name	Package Name	ATS Heat Sink	t-Global Thermal Pad
Mercury KX1	FBG676,FFG676 [20]	ATS-52270G-C1-R0	TG-A6200-28-28-1

Table 15: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

[4]The maximum available output current depends on your design. See sections 2.11.1 and 2.11.5 for details.

Warning!

Depending on the user application, the Mercury KX1 FPGA module may consume more power than can be dissipated without additional cooling measures; always make sure the FPGA is adequately cooled by installing a heat sink and/or providing air flow.

2.11.7 Voltage Monitoring

Several pins on the module connector on the Mercury KX1 FPGA module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 16 presents the VMON pins on the Mercury KX1 FPGA module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V0	A-102	VCC_INT	FPGA core voltage
VMON_1V2	B-167	VCC_1V2	1.2 V on-board voltage (default)/FPGA battery voltage (assembly option)
VMON_AUX_IO	B-168	VCC_2V0 on-board voltage (2.0 V for FFG packages, 1.8 V for FBG packages)	VCCAUX_IO voltage (required only for FFG packages)
VMON_1V5	B-8	VCC_DDR3	DDR3 voltage

Table 16: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.12 Clock Generation

A 100 MHz single-ended oscillator and a 200 MHz LVDS oscillator are equipped on the Mercury KX1 FPGA module. The 50 MHz clock for the Ethernet PHYs is generated from the 100 MHz system oscillator. The reference clock inputs for the MGT transceivers are available on the module connector pins.

Signal Name	Frequency	FPGA Pin	FPGA Pin Type	Remark
CLK100	100 MHz	AA3	IO_L12P_T1_MRCC_34	Main clock
CLK200_P CLK200_N	200 MHz	AC18 AD18	IO_L13P_T2_MRCC_32 IO_L13N_T2_MRCC_32	LVDS clock
FPGA_EMCCLK	100 MHz	B26	IO_L3N_T0_DQS_EMCCLK_14	External configuration clock

Table 17: Module Clock Resources

2.13 Reset

The FPGA configuration clear signal (FPGA_PROG#) and the FPGA delay configuration signal (FPGA_INIT#) of the Kintex-7 device are available on the module connector.

Pulling FPGA_PROG# low clears the FPGA configuration. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins and to the Xilinx documentation for details on the functions of the PROGRAM_B_0 and INIT_B_0 signals.

Table 18 presents the available reset signals. Both signals, FPGA_PROG# and FPGA_INIT#, have on-board 4.7 kΩ pull-up resistors to VCC_CFG_B13.

Signal Name	Connector Pin	FPGA Pin Type	Description
FPGA_PROG#	A-132	PROGRAM_B_0	Configuration clear signal
FPGA_INIT#	A-124	INIT_B_0	Delay configuration signal

Table 18: Reset Resources

FPGA_INIT# signal is also connected to a regular FPGA pin (FPGA_INIT#_R, package pin J14) via a 47 kΩ resistor and can be used to reset the FPGA logic. In this case, internal pull-up must not be used for this signal, in order to be able to reset the logic via FPGA_INIT# pin available on the module connector.

2.14 LEDs

Four LEDs are available on the Mercury KX1 FPGA module and they are connected to the FPGA logic. Another LED is connected to the Cypress FX3 USB 3.0 controller user pin for easy status signaling.

Table 19 shows the pin locations of the FPGA LEDs.

Signal Name	FPGA Pin	Remarks
LED0#	M17	User function/active-low
LED1#	L18	User function/active-low
LED2#	L17	User function/active-low
LED3#	K18	User function/active-low

Table 19: LEDs

2.15 DDR3 SDRAM

There are two independent DDR3 memory channels on the Mercury KX1 FPGA module: DDR3-A is 8 bits wide, while DDR3-B is 32 bits wide. Five identical 8-bit memory chips are used to build the entire memory sub-system.

The advantage of having two separate memory channels is that one of the memories can be used as an external memory for a soft processor like the Xilinx Microblaze, while the other can be used for high data rate transfers, for example in video processing applications.

Note that for FPGAs in FFG packages the memory interface supports speeds of up to 1600 Mb/s, while for devices in the FBG packages it supports up to 800 Mb/s.

The maximum memory bandwidth on the Mercury KX1 FPGA module is:

- *FFG package devices*: 1600 Mbit/sec × (32 + 8) bits = 8000 MB/sec
- *FBG package devices*: 800 Mbit/sec × (32 + 8) bits = 4000 MB/sec

Note that for DDR3 low power mode (DDR3L) the speed can be lower than mentioned above. For details, refer to the Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics [18].

2.15.1 DDR3 SDRAM Type

Table 20 describes the memory availability and configuration on the Mercury KX1 FPGA module.

Module	SDRAM Type	Density	Configuration	Manufacturer
ME-KX1-D10 (commercial)	MT41K256M8DA-125:K	2 Gbit	256 M × 8 bit	Micron
ME-KX1-D10 (commercial)	NT5CC256M8IN-DI	2 Gbit	256 M × 8 bit	Nanya
ME-KX1-D11 (industrial)	K4B4G0846D-BMK0	4 Gbit	512 M × 8 bit	Samsung
ME-KX1-D11 (industrial)	K4B4G0846E-BMMA	4 Gbit	512 M × 8 bit	Samsung
ME-KX1-D11 (industrial)	NT5CC512M8CN-DII	4 Gbit	512 M × 8 bit	Nanya
ME-KX1-D11 (industrial)	NT5CC512M8DN-DII	4 Gbit	512 M × 8 bit	Nanya
ME-KX1-D11 (industrial)	NT5CC512M8EN-DII	4 Gbit	512 M × 8 bit	Nanya
ME-KX1-D11 (industrial)	NT5CC512M8EQ-EKI	4 Gbit	512 M × 8 bit	Nanya
ME-KX1-D11 (industrial)	MT41K512M8RH-125IT:E	4 Gbit	512 M × 8 bit	Micron

Table 20: DDR3 SDRAM Types

Warning!

Other DDR3 memory devices may be equipped in future revisions of the Mercury KX1 FPGA module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

Please refer to the Mercury KX1 FPGA Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3 SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented for the data signals on the Mercury KX1 FPGA module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.15.4 Parameters

Please refer to the Mercury KX1 FPGA module reference design [2] for DDR3 settings guidelines. The DDR3 SDRAM parameters to be set in Vivado project are presented in Table 21. If the memory part equipped on the module is not available in Vivado, a custom memory part can be created and configured as described in the table.

The values given in Table 21 are for reference only. Depending on the equipped memory device on the Mercury KX1 FPGA module and on the DDR3 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory voltage	1.5 V (for DDR3)/1.35 V (for DDR3L)
Data width	8 bit (DDR3-A) and 32 bit (DDR3-B)
Clock period	1250 - 3300 ps (range depending on the FPGA package)
Bank address bits	3
Row address bits	15-16 (depending on the module type)
Column address bits	10
tcke	5 ns
tfaw	30.0 ns
tras	35 ns
trcd	13.75 ns
trefi	7.8 us
trfc	160 ns / 260 ns (depending on the module type)
trp	13.75 ns

Table 21: DDR3 SDRAM Parameters

2.15.5 DDR3 Low Voltage Operation

The default voltage of the DDR3 is 1.5 V. In order to enable low voltage mode (1.35 V), DDR3_VSEL (pin J8) must be driven logic 0 by the FPGA logic, and a memory voltage of 1.35 V must be selected in the Memory Interface Generator (MIG) parameters in Vivado.

For 1.5 V operation, DDR3_VSEL must be set to high impedance (not driven logic 1).

2.16 QSPI Flash

The QSPI flash can be used to store the FPGA bitstream, Microblaze application code and other user data.

2.16.1 QSPI Flash Type

Table 22 describes the memory availability and configuration on the Mercury KX1 FPGA module.

The bigger flash device introduced starting with revision 3 has bigger erase sectors (256 kB instead of 64 kB) and the 4 kB and 64 kB erase commands are not supported anymore. Further, the programming buffer is 512 bytes instead of 256 bytes. This may require adjustments of the programming algorithm.

Module	Flash Type	Size	Manufacturer
ME-KX1 - R1 and R2	N25Q256A13EF840F	256 Mbit	Micron
ME-KX1 - R3 and newer	S25FL512S	512 Mbit	Cypress (Spansion)

Table 22: QSPI Flash Types

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury KX1 FPGA module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.16.2 Signal Description

Signal Name	FPGA Pin Type	FPGA Pin	QSPI Pin Type Flash Pin	Module Connector Pin
FLASH_CLK_FPGA_CCLK	CCLK_0 IO_0_14	C8 K21	SCK	A-118
FLASH_CS#	IO_L6P_T0_FCS_B_14	C23	CS#	A-116
FLASH_DI	IO_L1P_T0_D00_MOSI_14	B24	SI/IO0	A-114
FLASH_DO_FPGA_DIN	IO_L1N_T0_D01_DIN_14	A25	SO/IO1	A-122
FLASH_WP#	IO_L2P_T0_D02_14	B22	WP#/IO2	-
FLASH_HOLD#	IO_L2N_T0_D03_14	A22	HOLD#/IO4	-

Table 23: QSPI Flash Interface

The QSPI flash is connected to the FPGA pins. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the FPGA and the flash device.

2.17 Dual Gigabit Ethernet

Two 10/100/1000 Mbit Ethernet PHYs are available on the Mercury KX1 FPGA module, connected to the FPGA via RGMII interfaces.

2.17.1 Ethernet PHY Type

Table 24 describes the equipped Ethernet PHY device type on the Mercury KX1 FPGA module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 24: Gigabit Ethernet PHY Type

2.17.2 Signal Description

The RGMII interfaces are connected to FPGA bank 13. The MDIO interface is shared between the two PHYs; these can be configured individually by using the corresponding addresses. Please refer to Section 2.17.4 for details.

The reset pin for the PHYs has a pull-down resistor and needs to be driven high to release the PHYs from reset.

The active low ETH_LED2# signals are connected to the FPGA as link indicators.

2.17.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.17.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY0 is 3, while the address assigned to PHY1 is 7. The MDIO interface is connected to the FPGA bank 13.

2.17.5 PHY Configuration

The configuration of the Ethernet PHYs is bootstrapped when the PHYs are released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 25.

Depending on the used IP core, configuration of the RGMII delays in the Ethernet PHYs may be required to achieve proper timing. For details on the RGMII delays, please refer to the PHY datasheet.

An example of PHY configuration is shown in the lwIP application provided in the Mercury KX1 FPGA module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011 111	PHY0: MDIO address 3 PHY1: MDIO address 7
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 25: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.18 Cypress FX3 USB 3.0 Controller

The Mercury KX1 FPGA module features a USB 3.0 controller from Cypress, which allows data transfers to a host computer using speeds of over 300 MB/s.

The USB controller is connected to the FPGA module using a slave FIFO interface that can be configured for 16-bit or 32-bit mode using an interface clock of 100 MHz. The USB 3.0 controller includes a 32-bit ARM926 core operating at 200 MHz using a 19.2 MHz crystal oscillator. It can access the I2C bus and the QSPI flash.

The Cypress FX3 JTAG interface can be routed to the optional JTAG connector J1500. Please refer to Section 3.4.3 for details.

2.18.1 Cypress FX3 Type

Table 26 describes the equipped Cypress FX3 controller type on the Mercury KX1 FPGA module.

Type	Manufacturer	Description
CYUSB3014	Cypress	USB 3.0 device controller (Cypress FX3) including USB 3.0 and USB 2.0 PHYs

Table 26: USB 3.0 Controller Type

2.18.2 Cypress FX3 Pinout

For details on FX3 interface pinout, please refer to the Mercury KX1 FPGA Module FPGA Pinout Excel Sheet [4] and Mercury KX1 FPGA Module User Schematics [5].

2.18.3 Functional Description

The FX3 controller is configured to boot from the FX3 SPI flash boot by default. The flash is factory programmed with a booloader that sets up all configuration pins of the FPGA correctly - if the FX3 bootloader is deleted or overwritten, the FPGA may not work correctly anymore.

Please make sure all configuration pins are properly setup if you load a custom FX3 firmware - in case a wrong firmware has been programmed to the FX3 SPI flash, the SPI flash boot can be prevented by shorting R1600 (see Figure 11).

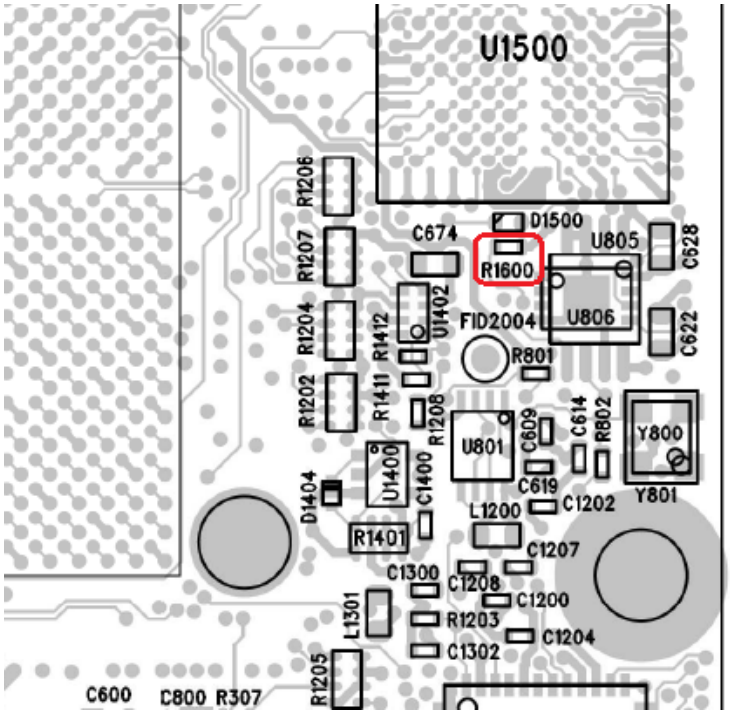

Figure 11: FX3 SPI Flash Boot Bypass - Assembly Drawing Top (middle right side) for Revision 4 Modules

For more information on the FPGA configuration pins, refer to Section 3.

2.19 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. The RTC features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus on the Mercury KX1 FPGA module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

Note that the frequency output mode of the RTC must be disabled when using I2C interrupt system. Otherwise, I2C_INT# is periodically pulled down by the RTC. The disabling of this function can be done by setting bits [3:0] of the RTC register 8 to logic low.

2.19.1 RTC Type

Table 27 describes the equipped RTC device type on the Mercury KX1 FPGA module.

Type	Manufacturer
ISL12020MIRZ	Intersil

Table 27: RTC Type

An example demonstrating how to use the RTC is included in the Mercury KX1 FPGA module reference design [2].

2.20 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.20.1 EEPROM Type

Table 28 describes the equipped EEPROM device type on the Mercury KX1 FPGA module.

Module	Type	Manufacturer
ME-KX1 - R1 and R2	DS28CN01	Maxim
ME-KX1 - R3 and newer	ATSHA204A-MAHDA-T (default)	Atmel
ME-KX1 - R3 and newer	DS28CN01 (assembly option)	Maxim

Table 28: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mercury KX1 FPGA module reference design [2].

3 Device Configuration

3.1 Configuration Signals

Table 29 describes the most important configuration pins.

Some of the pins are connected to a user I/O, as well as to a special purpose configuration pin. This is done for compatibility with other Mercury modules, on which the configuration pins can be used as user I/Os after configuration.

Signal Name	FPGA Pin Type	FPGA Pin	QSPI Flash Pin	Mod. Conn. Pin	Comments
FLASH_CLK_FPGA_CCLK	CCLK_0 IO_0_14	C8 K21	SCK	A-118	10 kΩ pull-up to VCC_CFG_B13
FLASH_CS#	IO_L6P_T0_FCS_B_14	C23	CS#	A-118	10 kΩ pull-up to VCC_CFG_B13
FLASH_DI	IO_L1P_T0_D00_MOSI_14	B24	SI/IO0	A-114	10 kΩ pull-up to VCC_CFG_B13
FLASH_DO_FPGA_DIN	IO_L1N_T0_D01_DIN_14	A25	SO/IO1	A-122	10 kΩ pull-up to VCC_CFG_B13
FPGA_INIT#	INIT_B_0 IO_25_16[5]	G7 J14	-	A-124	4.7 kΩ pull-up to VCC_CFG_B13
FPGA_DONE	DONE_0	J7	-	A-130	1 kΩ pull-up to VCC_CFG_B13
FPGA_PROG#	PROGRAM_B_0	P6	-	A-132	4.7 kΩ pull-up to VCC_CFG_B13

Continued on next page...

Signal Name	FPGA Pin Type	FPGA Pin	QSPI Flash Pin	Mod. Conn. Pin	Comments
FPGA_MODE	M1_0 M2_0	T2 P5	-	A-126	4.7 kΩ pull-up to VCC_CFG_B13
FPGA_CFGBVS	CFGBVS_0[6]	P7	-	-	10 kΩ pull-up to VCC_CFG_B13

Table 29: FPGA Configuration Pins

Warning!

All configuration signals except for FPGA_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped FPGA device, as well as other devices on the Mercury KX1 FPGA module.

3.2 Configuration Mode

The FPGA_MODE signals determine whether the FPGA device is configured from the QSPI flash or serially via SPI from an external device.

Table 30 describes the available configuration modes and the corresponding mode signals.

FPGA_MODE	Mode Straps [2:0]	Configuration Mode
0	001	Master serial configuration (boot from QSPI flash)
1	111	Slave serial configuration

Table 30: Configuration Modes

3.3 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to GND on the module; as PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R206 component and by mounting R205 - in this configuration the PUDC pin is connected to VCC_CFG_B13.

[5] FPGA_INIT# signal is connected to a regular FPGA pin via a 47 kΩ resistor.

[6] Note that the CFGBVS_0 (configuration bank voltage select) pin is set automatically to GND (if VCC_CFG_B13 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_B13 is 2.5 V or 3.3 V).

Figure 12 illustrates the configuration of the I/O signals during power-up. Figure 13 indicates the location of the pull-up/pull-down resistors on the module PCB - upper left part on the bottom view drawing.

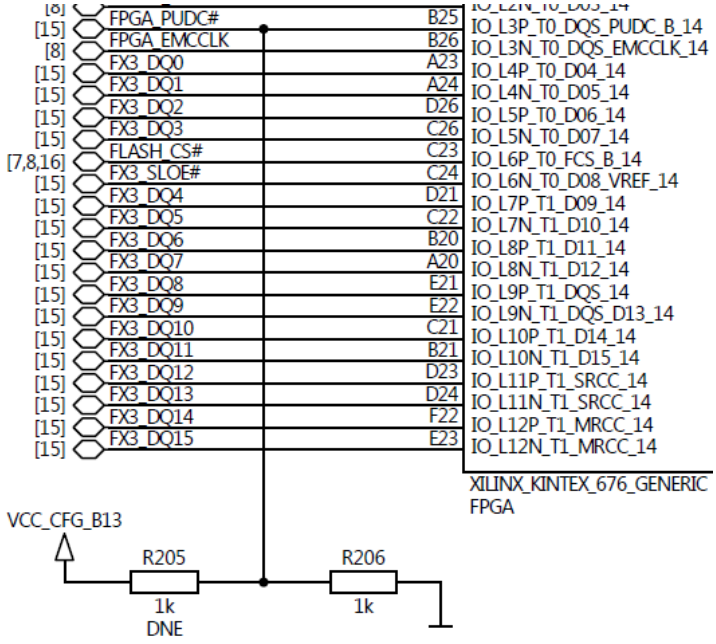

Figure 12: Pull-Up During Configuration (PUDC)

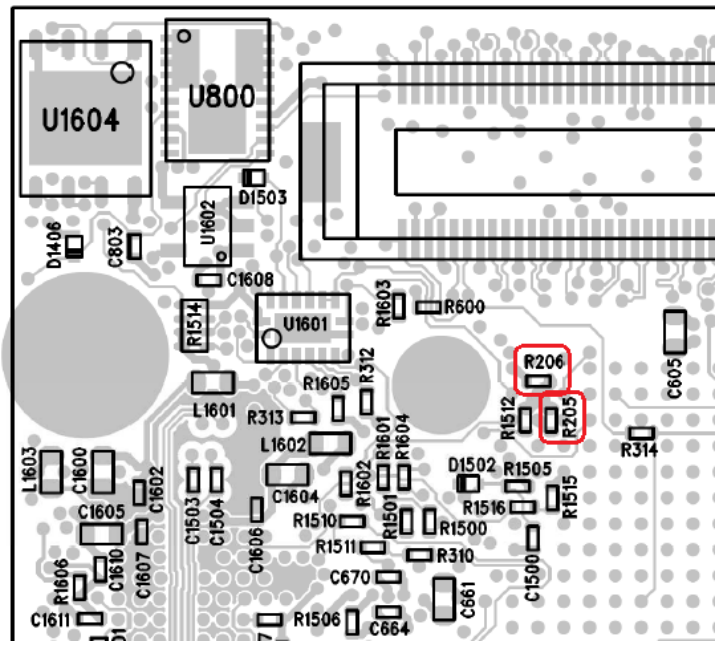

Figure 13: Pull-Up During Configuration (PUDC) Resistors - Assembly Drawing Bottom View (upper left corner) for Revision 4 Modules

For details on the PUDC signal please refer to the 7 Series FPGAs Configuration User Guide [17].

3.4 JTAG

The JTAG interface can be used for configuring and debugging the FPGA logic. The JTAG signals on the FPGA are directly connected to the module connector.

The FPGA device and the QSPI flash can be configured via JTAG using Xilinx tools.

3.4.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	A-123	4.7 kΩ pull-up to VCC_CFG_B13
JTAG_TMS	A-119	FPGA internal pull-up
JTAG_TDI	A-117	FPGA internal pull-up
JTAG_TDO	A-121	-

Table 31: JTAG Interface

3.4.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_B13.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.4.3 FX3 JTAG Connector

The Cypress FX3 JTAG interface are routed to the optional JTAG connector J1500. The FX3 TMS, TCK, TDI and TRST# pins have 4.7 kΩ pull-up resistors to VCC_3V3.

The FX3 JTAG connector type is Sullins GRPB052VWQS-RC.

3.5 Master Serial Configuration

In the master serial configuration mode, the FPGA reads the bitstream from the QSPI flash. The configuration clock can be configured up to 22 MHz and quad-SPI booting is supported. Higher configuration clocks can be achieved by using the advanced configuration settings of the Xilinx tools. For more information on the configuration modes, please refer to the 7 Series FPGAs Configuration User Guide [17].

3.5.1 Signal Description

Signal Name	Description
FLASH_CLK_FPGA_CCLK	Must be high impedance during configuration and operation
FLASH_DO_FPGA_DIN	Must be high impedance during configuration and operation
FPGA_INIT#	Is pulled low by the FPGA if any CRC error occurs during the configuration; it may be used as an input to delay the start of the FPGA configuration.
FPGA_DONE	Goes high after a successful FPGA configuration
FPGA_PROG#	When pulled low, the FPGA configuration sequence is cleared and all pins are tri-stated. The rising edge of FPGA_PROG# initializes the configuration.
FPGA_MODE	Must be pulled low during configuration
FLASH_DI	Must be high impedance during configuration and operation
FLASH_CS#	Must be high impedance during configuration and operation

Table 32: Master Serial Configuration - Signals Description

3.6 Slave Serial Configuration

In the slave serial configuration mode, the bitstream must be transmitted from an external device to the FPGA. The configuration pins of the FPGA are connected directly to the module connector, allowing the configuration of the FPGA from a microcontroller or another SPI capable device. For more information on the configuration modes, please refer to the 7 Series FPGAs Configuration User Guide [17].

For slave serial configuration the bitstream generation option “SPI_buswidth” must be set to 1 in the Xilinx tools.

3.6.1 Signal Description

Signal Name	Description
FLASH_CLK_FPGA_CCLK	Configuration clock
FLASH_DO_FPGA_DIN	Configuration data
FPGA_INIT#	Is pulled low by the FPGA if any CRC error occurs during the configuration; it may be used as an input to delay the start of the FPGA configuration.
FPGA_DONE	Goes high after a successful FPGA configuration
FPGA_PROG#	When pulled low, the FPGA configuration sequence is cleared and all pins are tri-stated. The rising edge of FPGA_PROG# initializes the configuration.
FPGA_MODE	Must be pulled high or left open during configuration

Table 33: Slave Serial Configuration - Signals Description

Warning!

Note that after the rising edge of FPGA_DONE, the FPGA still requires a number of clock cycles to finish the configuration. Therefore, if the FPGA_CCLK and FPGA_DIN pins are used in the FPGA design, the user must ensure that these are tri-stated by the FPGA logic for the appropriate amount of time. Details on the configuration time are available in Xilinx AR #42128.

3.7 QSPI Flash Programming via JTAG

The Xilinx Vivado and SDK software offer QSPI flash programming support via JTAG. For more information, please refer to the Xilinx Documentation [19].

To use quad-mode for the SPI flash, the bitstream generation option "SPI_buswidth" must be set to 4 in the Xilinx tools. In addition, the SPI flash must be configured to 4-bit mode when programming the flash.

3.8 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the FPGA device as well, the FPGA device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the FPGA_PROG# to GND, which puts the FPGA device into reset state and tri-states all I/O pins during flash programming.

Figure 14 shows the signal diagrams corresponding to flash programming from an external master.

To use quad-mode for the SPI flash, the bitstream generation option "SPI_buswidth" must be set to 4 in the Xilinx tools. In addition, the SPI flash must be configured to 4-bit mode by the programmer.

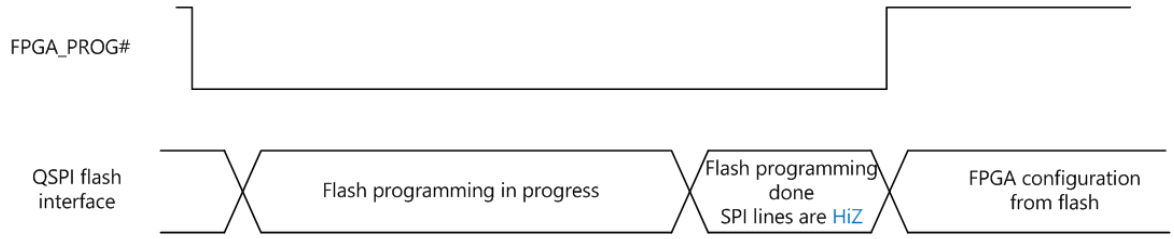

Figure 14: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the FPGA device into reset may damage the equipped FPGA device, as well as other devices on the Mercury KX1 FPGA module.

3.8.1 Signal Description

Signal Name	QSPI Flash Pin	Description
FLASH_CLK_FPGA_CCLK	SCK	SPI CLK
FLASH_DO_FPGA_DIN	SO/IO1	SPI MISO
FPGA_PROG#	-	Must be pulled low during QSPI flash programming. When released, all other pins of the SPI interface must be high impedance.
FLASH_DI	SI/IO0	SPI MOSI
FLASH_CS#	CS#	SPI CS#

Table 34: Flash Programming from an External Master - Signals Description

3.9 Enclustra Module Configuration Tool

The QSPI flash on the Mercury KX1 FPGA module can be programmed via Cypress FX3 using the Enclustra Module Configuration Tool (MCT) [14]. Slave serial configuration is also supported by the Enclustra MCT software.

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury KX1 FPGA module is connected to the FPGA device, EEPROM, RTC and FX3 USB 3.0 controller, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

Please note that the RTC must be configured correctly to use I2C interrupts - for details, refer to Section 2.19.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 35 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the FPGA and must not be driven from the FPGA device.

Level shifters are used between the I2C bus and the FPGA pins, to allow I/O voltages lower than 3.3 V.

Signal Name	FPGA Pin	Connector Pin	Resistor
I2C_SDA	P24	A-113	2.2 kΩ pull-up
I2C_SCL	N24	A-111	2.2 kΩ pull-up
I2C_INT#	N19	A-115	10 kΩ pull-up

Table 35: I2C Signal Description

4.3 I2C Address Map

Table 36 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.20)
0x57	RTC user SRAM
0x6F	RTC registers

Table 36: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury KX1 FPGA module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 37: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury KX1 FPGA module	0x0325	0x[XX]	0x[YY]	0x0325 [XX][YY]

Table 38: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	FPGA Type	0	5	See FPGA type table (Table 40)
	3-0	FPGA device speed grade	1	3	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low Power)	
	5-4	Ethernet port count	0	2	
	3	Ethernet speed	0 (Fast)	1 (Gigabit)	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 3.0 device port count	0	1	
0x0B	7-4	Primary DDR3 RAM size (MB)	0 (0 MB)	9 (2 GB)	Resolution = 8 MB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	7-4	Reserved	-	-	
	3-0	Secondary DDR3 RAM size (MB)	0 (0 MB)	9 (512 MB)	Resolution = 2 MB

Table 39: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 40 shows the available FPGA types.

Value	FPGA Device Type
0	XC7K160T, FBG package
1	XC7K325T, FBG package
2	XC7K410T, FBG package
3	XC7K160T, FFG package
4	XC7K325T, FFG package
5	XC7K410T, FFG package

Table 40: FPGA Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 41 indicates the absolute maximum ratings for Mercury KX1 FPGA module. The values given are for reference only; for details please refer to the Kintex-7 Datasheet [18].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 41: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 42 indicates the recommended operating conditions for Mercury KX1 FPGA module. The values given are for reference only; for details please refer to the Kintex-7 Datasheet [18].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 42: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

References

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