Mercury+ MP1 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ MP1 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ MP1 SoC module.

Summary

This document first gives an overview of the Mercury+ MP1 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-MP1	Mercury+ MP1 SoC Module

Document Information	Reference	Version	Date
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Approval Information	Name	Position	Date
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Verified by	MMOS, GKOE	Design Expert	26.01.2023
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Document History

Version	Date	Author	Comment
01	16.02.2023	WRUH, ABUE, SKOS	Version 01

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1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ MP1 SoC module combines the Microchip Polarfire® SoC (System-on-Chip) device with PCIe® Gen2 ×4, one USB 2.0 PHY (with OTG support), up to two Gigabit Ethernet PHYs, DDR4 SDRAM with Error Correction Code (ECC), eMMC flash, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mercury+ MP1 SoC module, in contrast to building a custom SoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mercury+ base boards, the Mercury+ MP1 SoC module allows the user to quickly build a system prototype and start with application development.

A Yocto layer is available for the Mercury+ MP1 SoC module. This layer allows the user to quickly build and run linux on the Mercury+ MP1 SoC module.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA permanent lock-bits are modified. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mercury+ MP1 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury+ MP1 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ MP1 SoC module.

1.1.5 Safety Recommendations and Warnings

Mercury+ modules are not designed to be “ready for operation” for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury+ MP1 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ MP1 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Microchip PolarFire SoC
  - MPFS250T/MPFS460T device
  - FCG1152 package
  - Four 64-bit RV64GC Quad Application processing cores up to 625 MHz
  - 64-bit RV64IMAC monitor processor core up to 625 MHz
  - Non-volatile FPGA fabric (28 nm process technology)
- *MPFS250T:* 215 user I/Os
  - 208 IOs (up to 3.3 V)
  - 9 MSS I/Os
- *MPFS460T:* 195 user I/Os
  - 188 IOs (up to 3.3 V)
  - 9 MSS I/Os
- 20 MGTs @ 12.7 Gbit/sec (MPFS460T -1 speed grade) and 10 reference input clock differential pairs
- 16 MGTs @ 10.3125 Gbit/sec (MPFS250T STD speed grade) and 8 reference input clock differential pairs
- PCIe Gen2 ×4 support
- Up to 4 GB DDR4 SDRAM with ECC on MSS side
- Up to 8 GB DDR4 SDRAM on FPGA side
- 64 MB quad SPI flash
- 64 MB SPI flash
- 16 GB eMMC flash
- Up to 2 × Gigabit Ethernet (SGMII interface on MSS side)
- USB 2.0 OTG
- Real-time clock
- UART, SPI, I2C, SDIO/MMC
- 5 to 13.2 V single supply

1.3 Deliverables

- Mercury+ MP1 SoC module
- Mercury+ MP1 SoC module documentation, available via download:
  - Mercury+ MP1 SoC Module User Manual (this document)
  - Mercury+ MP1 SoC Module Reference Design [2]
  - Mercury+ MP1 SoC Module IO Net Length Excel Sheet [3]
  - Mercury+ MP1 SoC Module FPGA Pinout Excel Sheet [4]
  - Mercury+ MP1 SoC Module User Schematics (PDF) [5]
  - Mercury+ MP1 SoC Module Known Issues and Changes [6]
  - Mercury+ MP1 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mercury+ MP1 SoC Module 3D Model (PDF) [8]
  - Mercury+ MP1 SoC Module STEP 3D Model [9]
  - Mercury Mars Module Pin Connection Guidelines [10]
  - Mercury Master Pinout [11]

- Mercury Heatsink Application Note [19]
- Yocto BSP Layer for Enclustra modules equipped with Microchip SoCs [16]
- Custom Hart Software Services for Enclustra modules [17]

1.3.1 Reference Design

The Mercury+ MP1 SoC module reference design features an example configuration for the PolarFire SoC device, together with an example top level HDL file for the user logic.

A "hello world" bare-metal software application is available to provide a starting point for own user applications. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

A custom version of the Hart Software Services [17] contains all required modifications to initialize the microprocessor subsystem and to allow booting Linux or user applications.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.3.2 Yocto BSP

The Enclustra Yocto BSP Layer [16] enables the user to quickly set up a Yocto project and to run Linux on the Enclustra SoC module.

The documentation describes the build process in detail and allows a user without Yocto knowledge to build and run a Linux reference design on the target hardware.

1.4 Accessories

1.4.1 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.10.6 for further information on the available cooling options.

1.4.2 Mercury+ PE1 Base Board

The Mercury+ PE1 is a versatile PCIe® x4 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.
It is compatible with a multitude of FMC boards from different suppliers to use in data acquisition systems, motor control, display and camera interfaces, software defined radio and more. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

For more information visit
`https://www.enclustra.com/en/products/base-boards/mercury-pe1-200-300-400/`.

Please note that the available features depend on the Mercury module type and on the selected base board variant.

1.4.3 Mercury+ PE3 Base Board

The Mercury+ PE3 is a versatile PCIe® x8 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.
This high performance base board provides a versatile set of I/O connectivity options, specialized for high-speed communication and video applications, including SFP+, QSFP+, HDMI, USB Type-C and Firefly. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom

hardware.

For more information visit `https://www.enclustra.com/en/products/base-boards/mercury-pe3/`.

Please note that the available features depend on the Mercury module type and on the selected base board variant.

1.4.4 Mercury+ ST1 Base Board

The Mercury+ ST1 board is a compact, low-cost base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules.
It provides a versatile set of I/O connectivity options, specialized for video applications, including MIPI, HDMI and SFP+. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

For more information visit `https://www.enclustra.com/en/products/base-boards/mercury-st1/`.

Please note that the available features depend on the Mercury module type and on the selected base board variant.

1.5 Microchip Tool Support

The SoC devices equipped on the Mercury+ MP1 SoC module are supported by the Microchip Libero SoC Design Suite software. A platinum license is required (support for S devices). Please contact Microchip for further information.

2 Module Description

2.1 Block Diagram

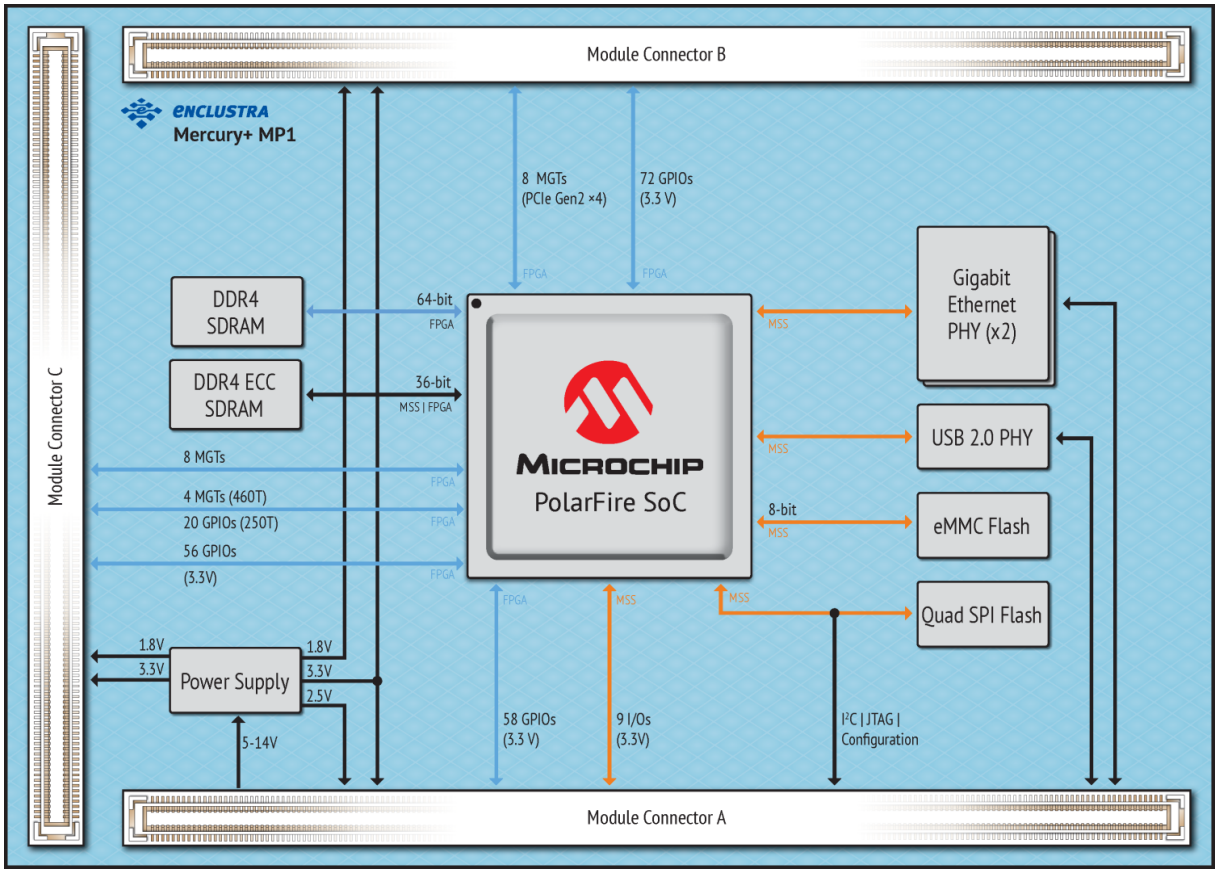

Figure 1: Hardware Block Diagram

The main component of the Mercury+ MP1 SoC module is the Microchip PolarFire SoC device. Most of its I/O pins are connected to the Mercury+ module connector, making up to 215 regular user I/Os available to the user. Further, up to 20 MGT pairs are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen2 ×4.

Mercury+ MP1 SoC modules equipped with MPFS460 SoC devices have a different amount of XCVR transceivers and GPIOs compared to a Mercury+ MP1 SoC modules equipped with a MPFS250 SoC device. The difference between these assembly variants is described in detail in section 2.8.2.

The FPGA is flash based and is configured almost instantly after reset is released. Alternatively the device supports loading the bitstream from SPI flash. The RISC-V processor subsystem of the Polarfire SoC allows booting from the internal flash memory. The reference design supports booting Linux from SD Card and eMMC memory. For development purposes, a JTAG interface is connected to Mercury module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash, a 64 MB SPI flash, up to 4 GB DDR4 SDRAM with ECC connected to the MSS and up to 8 GB DDR4 SDRAM connected to the FPGA.

Further, the module can be equipped with up to two Gigabit Ethernet PHYs and one USB 2.0 PHY, making it ideal for communication applications.

A real-time clock is available on the Mercury+ MP1 SoC module.

All clock signals which are required for the components equipped, are generated on the module. This includes a 125 MHz differential clock for the SGMII and MSS clocking and a 50 MHz FPGA fabric clock.

The module's internal supply voltages are generated from a single input supply of 5 - 13.2 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Four LEDs are connected to the SoC pins for status signaling.

2.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Model	SoC	DDR4 ECC SDRAM (MSS)	DDR4 SDRAM (FPGA)	Temperature Range
ME-MP1-250-SI-D3EN-E1	MPFS250TS-FCG1152I	2 GB	N/A	-40 to +85° C
ME-MP1-460-1SI-D4E-E1	MPFS460TS-1FCG1152I	4 GB	8 GB	-40 to +85° C

Table 1: Standard Module Configurations

The product model indicates the module type and main features. Figure 2 describes the fields within the product model.

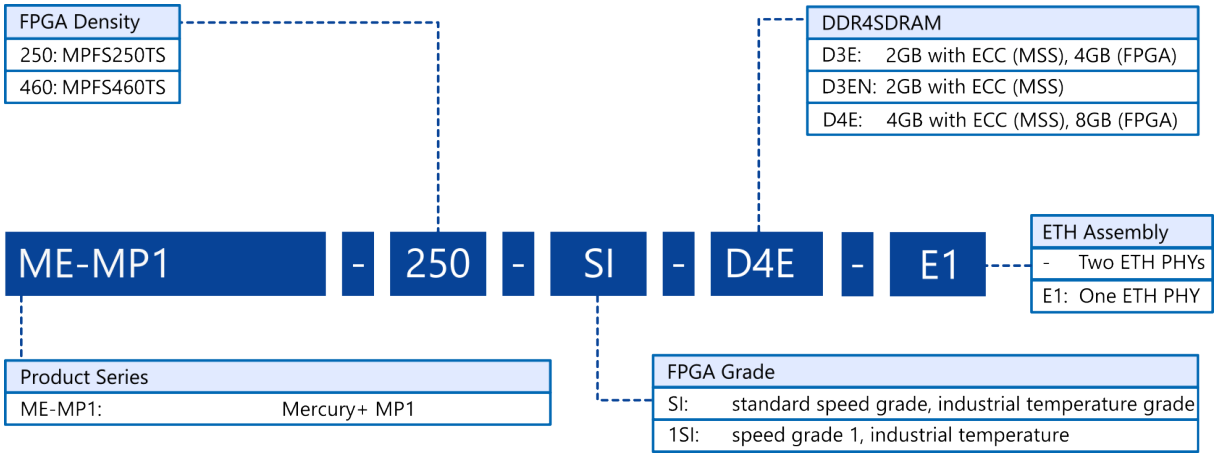

Figure 2: Product Model Fields

Please note that for the first revision modules or early access modules, the product model may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 EN-Numbers and Product Models

Every module is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

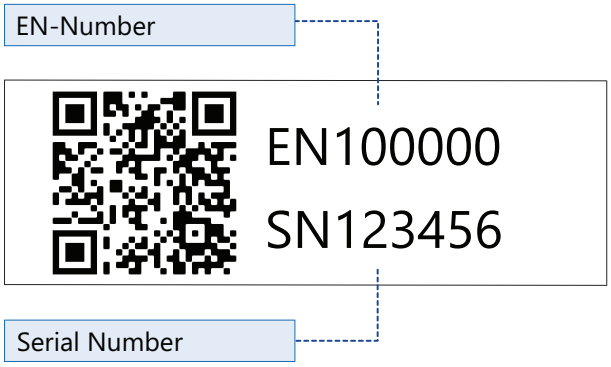

Figure 3: Module Label

The correspondence between EN-number and product model for each revision is shown in Table 2.

The revision changes and product known issues are described in the Mercury+ MP1 SoC Module Known Issues and Changes document [6].

EN-Number	Product Model	Revision Number
EN105249	ME-MP1-250-SI-D3EN-E1	R1.0
EN105251	ME-MP1-460-1SI-D4E-E1	R1.0

Table 2: EN-Numbers and Product Models

2.4 Top and Bottom Views

2.4.1 Top View

Figure 4: Module Top View

2.4.2 Bottom View

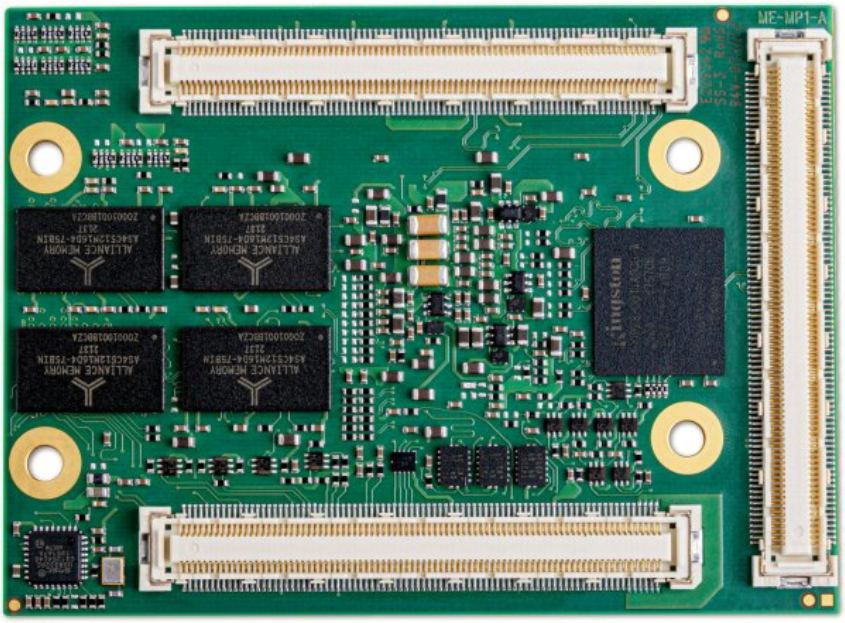

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

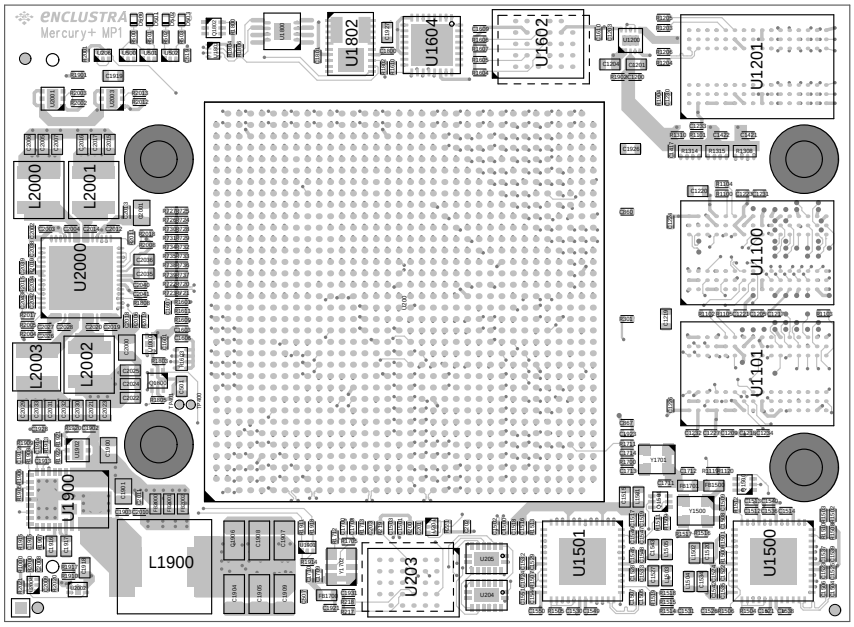

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

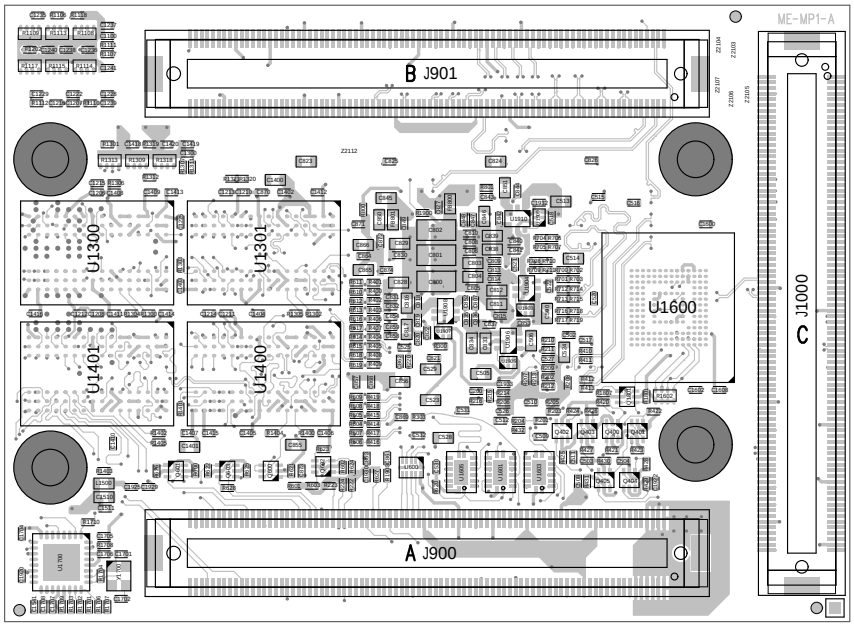

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint and Mechanical Data

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height under the module is dependent on the connector type - refer to Section 2.7 for detailed connector information.

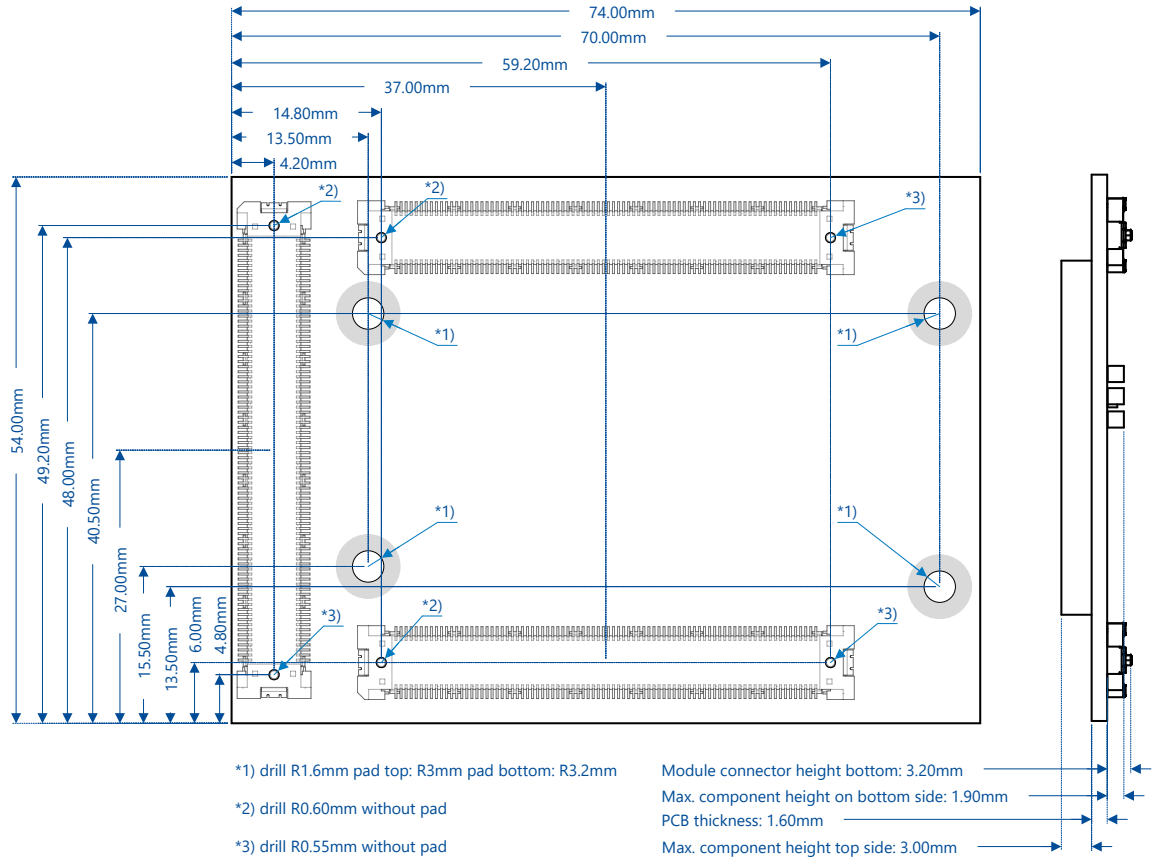

Figure 8: Module Footprint and Dimensions - Top View and Side View

Warning!

It is possible to mount the Mercury+ MP1 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ MP1 SoC module.

Table 3 describes the mechanical characteristics of the Mercury+ MP1 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Parameter	Value
Size	74 × 54 mm
Component height top	3.00 mm
Component height bottom	1.9 mm
Weight	36 g

Table 3: Mechanical Data

2.7 Module Connector

Three Hirose FX10 168-pin 0.5 mm pitch headers with a total of 504 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Types

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J900-1 to J900-168
- Connector B: from J901-1 to J901-168
- Connector C: from J1000-1 to J1000-168

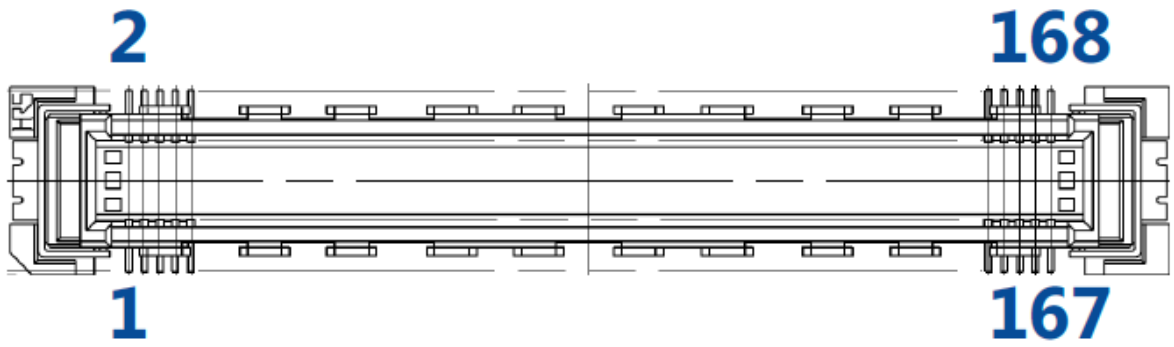

Figure 9: Pin Numbering for the Module Connector

Warning!

Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.

2.8 User I/O

2.8.1 Pinout

Information on the Mercury+ MP1 SoC module pinout can be found in the Enclustra Mercury Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury+ MP1 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, XCVR signals, etc).

The naming convention for the user I/Os located on GPIO banks is:
GPIO_B<BANK>_T<GROUP>_L<PAIR><_SPECIAL_FUNCTION>_<POLARITY>.

For example, GPIO_B1_T3_L4_CLKIN_P is pair 4 of group 3 and is connected to FPGA GPIO bank 1. It has positive polarity if used as a differential pair with the special function of a preferred clock input.

IO_B1_C8_LS and BOOT_MODE_LS are an exception and do not follow this naming convention. It is connected through a level shifter to GPIO Bank 1. It is also separately mentioned in chapter 2.8.2.

The naming convention for the user I/Os located on HSIO banks is:
IO_B<BANK>_<PIN_NAME>_<SPECIAL_FUNCTION>.

For example, IO_B8_AN4_UARTRX is connected to FPGA HSIO bank 8, is connected to the SoC at pin AN4 and can be used for an UART interface.

FPGA_DONE_LS is an exception and does not follow this naming convention. It is connected through a level shifter to HSIO Bank 0. It is also separately mentioned in chapter 2.8.2.

Further special functions are listed in the Polarfire SoC FPGA Packaging and Pin Descriptions [22].

Table 5 lists information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Sign.	Pairs	Differential	Single-ended	I/O Bank
GPIO_B1_<...>	56	28	In/Out	In/Out	GPIO Bank 1
IO_B1_C8_LS	1	0	In/Out	In/Out	GPIO Bank 1
BOOT_MODE	1	0	In/Out	In/Out	GPIO Bank 1
GPIO_B7_<...>	50	25	In/Out	In/Out	GPIO Bank 7
GPIO_B9_<...>	92 (MPFS250) 72 (MPFS460)	46 (MPFS250) 36 (MPFS460)	In/Out	In/Out	GPIO Bank 9
IO_B0_<...>	5	0	In/Out	In/Out	HSIO Bank 0
FPGA_DONE_LS	1	0	In/Out	In/Out	HSIO Bank 0
IO_B8_<...>	2	0	In/Out	In/Out	HSIO Bank 8

Table 5: User I/Os

The multi-gigabit transceiver (XCVR) are described in section 2.9.

2.8.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

UART interface

Table 6 lists the I/O pin exceptions on the Mercury+ MP1 SoC module related to the UART interface which is connected via a level shifter.

I/O Name	Module Connector Pin	SoC Connection	Connector Voltage Level	SoC Voltage Level
IO_B8_AN4_UARTRX	A-105	HSIO Bank 8 (Pin AN4)	VCC_CFG	VCC_1V2
IO_B8_AP4_UARTTX	A-107	HSIO Bank 8 (Pin AP4)	VCC_CFG	VCC_1V2

Table 6: I/O Pin Exceptions - UART interface

Both signals have a level of VCC_CFG on the connector and are connected to the FPGA via a level shifter to 1.2 V.

I/O Pins with Level Shifter

There are five signals on the Mercury+ MP1 SoC module that are routed from the FPGA banks to the module connector via level shifters - these are presented in Table 7.

I/O Name	Module Connector Pin	Connector voltage level	SoC voltage level
IO_B0_AN26_LS	A-88	VCC_CFG	VCC_1V2
IO_B0_AN27_LS	A-90	VCC_CFG	VCC_1V2
IO_B0_AL25_LS	A-92	VCC_CFG	VCC_1V2
IO_B0_AM24_LS	A-94	VCC_CFG	VCC_1V2
IO_B1_C8_LS	A-110	VCC_CFG	VCC_IO_B1
BOOT_MODE_LS	A-112	VCC_CFG	VCC_IO_B1
FPGA_DONE_LS	A-130	VCC_CFG	VCC_1V2
IO_B0_AE25_PERST#_LS	A-104	VCC_CFG	VCC_1V2

Table 7: I/O Pin Exceptions - Level Shifters

The level shifters used for signals IO_B0_AN26_LS, IO_B0_AN27_LS, IO_B0_AL25_LS and IO_B0_AM24_LS are NXP NTB0104 and the maximum achievable data rate on these pins is 30 Mbit/sec. The signal level of IO_B1_C8_LS is shifted by a EM6K34 MOSFETs.

Assembly Options

The number of user I/Os and XCVRs available on the module connector depends on the SoC device assembled on the Mercury+ MP1 SoC module.

On the Mercury+ MP1 SoC modules equipped with the bigger SoC device (MPFS460), there are four XCVR transceiver lines with two differential clock inputs more available than on the Mercury+ MP1 SoC modules equipped with the smaller SoC device (MPFS250). Mercury+ MP1 SoC modules equipped with the smaller SoC device (MPFS250) have 20 GPIOs more instead.

The diagram shown in figure 10 shows how the shared signals on connector C are connected via resistor assembly options to the FPGA for the two different SoC devices.

Design support files such as the Mercury Master Pinout [11], Mercury+ MP1 SoC Module User Schematics [5], and Mercury+ MP1 SoC Module FPGA Pinout Assembly Variants Excel Sheet [20] offer additional information on assembly options. In the user schematics, this information is depicted in the "Assembly Variants" section at the end of the PDF file.

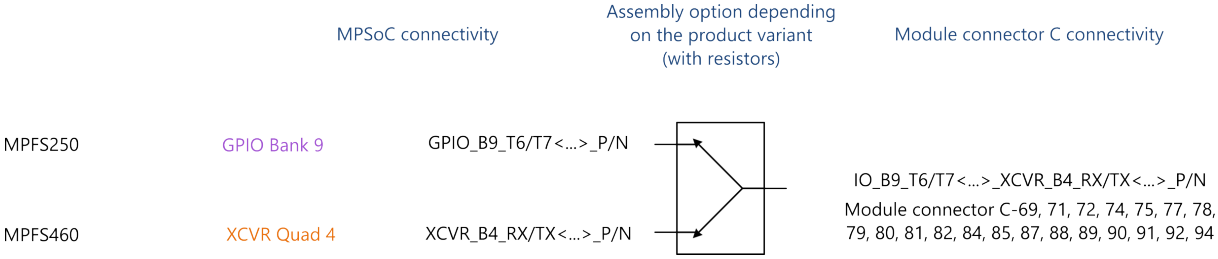

Figure 10: Signal connection for different SoC types.

Additionally, there are 10 GPIOs (GPIO_B1_T3_L[1-5]_P/N) on the module connector that are connected to GPIO Bank 1. If the Mercury+ MP1 SoC module is equipped with a MPFS460 SoC device, these signals are additionally routed to HSIO Bank 0 via a 49.9 Ω resistor.

2.8.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mercury+ MP1 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mercury+ MP1 SoC module. Please use the information provided in the Mercury+ MP1 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

While GPIO pins have an internal 100 Ω differential termination resistor that can be enabled in the Libero SoC software, HSIO pins need external termination.

Warning!

Check Mercury+ MP1 SoC module pinout with Libero SoC before producing your own base board hardware, to make sure that all pins are used according to the correct direction.

2.8.4 I/O Banks

Table 8 describes the main attributes of the Programmable Logic (FPGA) and Microprocessor Subsystem (MSS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O voltage (VCC_IO).

Bank	Connectivity	VCC_IO
MGT (XCVR) Bank 0	Module connector	1.05 V
MGT (XCVR) Bank 1	Module connector	1.05 V
MGT (XCVR) Bank 2	Module connector	1.05 V
MGT (XCVR) Bank 3	Module connector	1.05 V
MGT (XCVR) Bank 4	Module connector	1.05 V
FPGA HSIO Bank 0	FPGA DDR4 SDRAM, module connector	1.2 V
FPGA HSIO Bank 8	FPGA DDR4 SDRAM, clock oscillator, module connector	1.2 V
FPGA GPIO Bank 1	Module connector, I2C, Ethernet PHY GPIO	User selectable VCC_IO_B1
FPGA GPIO Bank 7	Module connector, TPM, Power Synchronization	User selectable VCC_IO_B7

Continued on next page...

Bank	Connectivity	VCC_IO
FPGA GPIO Bank 9	Module connector, LEDs	User selectable VCC_IO_B9
MSS Bank 2	I2C, QSPI, LEDs, MDIO, USB	VCC_3V3_SEQ
MSS Bank 4	SDIO, eMMC	VCC_CFG
MSS Bank 5	SGMII (Ethernet)	VCC_3V3_SEQ
MSS DDR Bank 6	MSS DDR4 SDRAM	1.2 V
Bank 3 (Configuration)	JTAG, SPI Flash, External SPI master	VCC_CFG

Table 8: I/O Banks

2.8.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	SoC Pins	Supported Voltages	Connector A Pins	Connector B Pins	Connector C Pins
VCC_CFG	VDDI3, VDDI4	1.8 V - 3.3 V ±5%	74, 77	-	-
VCC_IO_B7	VDDI7	1.8 V - 3.3 V ±5%	38, 41	-	-
VCC_IO_B9	VDDI9	1.2 V - 3.3 V ±5%	-	64, 67, 88, 95, 140, 143	-
VCC_IO_B1	VDDI1	1.2 V - 3.3 V ±5%	-	-	76, 116, 158

Table 9: VCC_IO Pins

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mercury+ MP1 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mercury+ MP1 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 11 illustrates the VCC_IO power requirements.

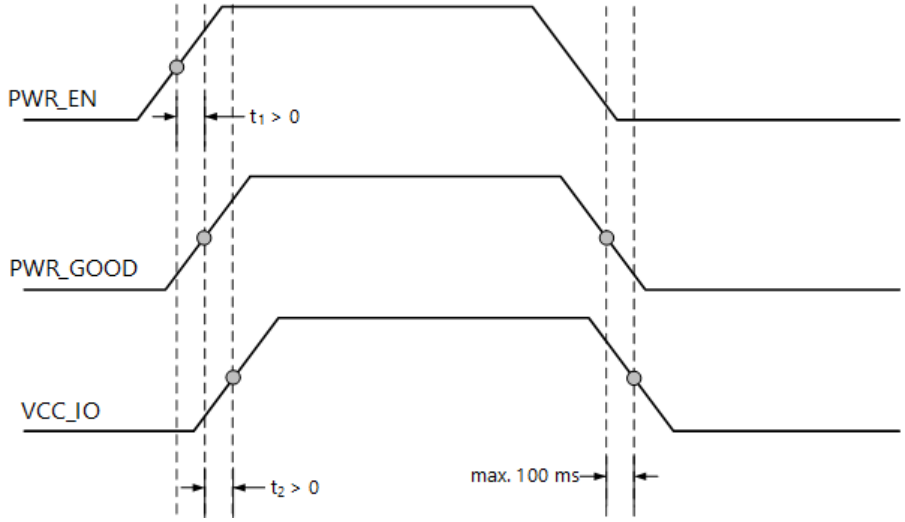

Figure 11: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.8.6 Signal Terminations

Differential I/Os

There are no external differential termination resistors on the Mercury+ MP1 SoC module for differential I/Os. These pairs may be terminated by external termination resistors on the base board (close to the module pins).

For available on-die differential termination resistors please refer to the PolarFire FPGA and SoC FPGA User I/O User Guide [25].

Single-Ended I/Os

There are external 49.9 Ω series termination resistors on some signals These resistors are required for the implementaion of MIPI interfaces. For details please refer to the PolarFire SoC FPGA Board Design Guidelines [24] and the user schematics [5].

For available on-die differential termination resistors please refer to the PolarFire FPGA and SoC FPGA User I/O User Guide [25].

2.8.7 MSS I/O Pins

Table 10 gives an overview over the MSS I/O pin connections on the Mercury+ MP1 SoC module.

Pins	Function	Connection
0-6	eMMC flash, SD card	eMMC, SD card
7-8	eMMC flash, user functionality	eMMC, external user functionality via multi-plexer
9	eMMC flash, SD card	eMMC, SD card
10-11	eMMC flash, user functionality	eMMC, external user functionality via multi-plexer
12	MSS reset (MSS_RST#)	SPI Flash, Ethernet PHY(s), USB PHY, QSPI and eMMC flash reset
13	I2C interrupt	Module connector via level shifter
14-25	USB	USB 2.0 PHY
26-27	I2C	Module connector via level shifter
28-29	Ethernet MDIO	Gigabit Ethernet PHY 0 and 1
30-35	QSPI flash	QSPI flash
36-37	LED0#, LED1#	On-board LEDs via buffer

Table 10: MSS I/O Pins Connections Overview

2.9 Multi-Gigabit Transceiver (XCVR)

The multi-gigabit transceivers on the Mercury+ MP1 SoC module are referred to as XCVR which are all connected to the FPGA of the SoC.

There are 16 XCVR transceivers available which are organized in four quads.

8 XCVR pairs and two corresponding clocks are routed to module connector B and C respectively. Resulting in a total amount of 16 XCVR pairs (64 XCVR signals) and 8 clocks (16 XCVR clock signals) available on the module connectors.

Aditionally, modules equipped with a MPFS460T device have a fifth quad available on connector C. Other devices have GPIOs on these connector pins - Table 11 describes the connections.

Signal Name	Signal Description	Pairs	Quad	Comment
XCVR_B0_RX<...>	MGT receivers	4	0	-
XCVR_B0_TX<...>	MGT transmitters	4		
XCVR_B0_REFCLK[A,B]<...>	MGT reference input clocks	2		
XCVR_B1_RX<...>	MGT receivers	4	1	-
XCVR_B1_TX<...>	MGT transmitters	4		

Continued on next page...

[0]Used for PCIe PERST# connection implementation. Refer to Section 2.8.2 for details.
[1]UART RX is an SoC input; UART TX is an SoC output.

Signal Name	Signal Description	Pairs	Quad	Comment
XCVR_B1_REFCLK[A,B]<...>	MGT reference input clocks	2		
XCVR_B2_RX<...>	MGT receivers	4	2	-
XCVR_B2_TX<...>	MGT transmitters	4		
XCVR_B2_REFCLK[A,B]<...>	MGT reference input clocks	2		
XCVR_B3_RX<...>	MGT receivers	4	3	-
XCVR_B3_TX<...>	MGT transmitters	4		
XCVR_B3_REFCLK[A,C]<...>	MGT reference input clocks	2		
XCVR_B4_RX<...>	MGT receivers	4	4	Only on MPFS460 devices
XCVR_B4_TX<...>	MGT transmitters	4		
XCVR_B4_REFCLK[A,B]<...>	MGT reference input clocks	2		

Table 11: XCVR Pairs

The naming convention for the XCVR MGT I/Os is:
XCVR_B<QUAD_NUMBER>_<FUNCTION><PAIR_NUMBER_LETTER>_<POLARITY>.

For example, XCVR_B1_RX0_P is the first receiver signal of quad 1 with positive polarity.

The XCVR signals on a standard speed grade SoC device support data rates of up to 10.3125 Gbit/sec whereas devices with speed grade -1 support data rates of up to 12.7 Gbit/sec.

The SoC devices equipped on the Mercury+ MP1 SoC module can support up to one integrated PCIe Gen3 ×4 interfaces on the FPGA fabric, implemented using XCVR transceivers. This interface is only available within quad 0. For more information please refer to the PolarFire FPGA and PolarFire SoC FPGA PCI Express User Guide [21].

Warning!

It is recommended to use redrivers on the base board for PCIe Gen2 or other high-speed interfaces implementations, and to perform channel simulation.

Warning!

The maximum data rate on the XCVR lines on the Mercury+ MP1 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using XCVRs at high performance rates.

Warning!

No AC coupling capacitors are placed on the Mercury+ MP1 SoC module on the XCVR lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent XCVR lines from being damaged.

2.10 Power

2.10.1 Power Generation Overview

The Mercury+ MP1 SoC module uses a 5 - 13.2 V DC power input for generating the on-board supply voltages (1.05/1 V, 1.2 V, 1.8 V, 2.2 V, 2.5 V, 3.3 V and 5.0 V). Some of these voltages (1.8 V, 2.5 V, 3.3 V) are accessible on the module connector.

Table 12 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_VDD	1.05/1 V (Core power supply)	20 A	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	4 A	VCC_MOD	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_MOD	Yes	Yes
VCC_2V5	2.5 V	2 A	VCC_MOD	Yes	Yes
VCC_3V3	3.3 V	4 A	VCC_MOD	No	Yes
VREF_2V2	2.2 V	0.5 A	VCC_2V5	Yes	Yes
VCC_3V3_PI	3.3 V	0.05 A	VCC_MOD	No	No
VCC_5V0_IRPS	5.0 V	0.05 A	VCC_MOD	No	No
VCC_5V0_IR	5.0 V	0.05 A	VCC_MOD	No	No

Table 12: Generated Power Supplies

In the standard configuration the core power supply is 1.05 V. For custom configurations this voltage can be changed to 1 V.

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

Power Converter Synchronization

All switching DC/DC converters used on the Mercury+ MP1 SoC module support synchronization of the switching frequency with an external clock. The module includes a power synchronization circuit, which may drive a clock generated by the SoC device to all the DC/DC converters.

By default, the free-running switching frequency of the DC/DC converters is set. To set the switching frequency to a desired value, a clock must be generated on SoC pin M6 of bank 7. Table 13 presents the control signal for the power converter synchronization.

Signal	SoC Pin	Description
PWR_SYNC	Package pin M6	Clock signal used for DC/DC converters synchronization • Connect to GND or leave floating if power synchronization is not needed. • Clock signal: The DC/DC converters are synchronized with this external clock signal.

Table 13: Power Converter Synchronization

The synchronization frequency valid for all switching DC/DC converters on-board and compensation networks must lie in the range of 600 kHz ±3% for the whole operating temperature range of -40 to 125 °C. For a temperature range of 0 to 85 °C this frequency range increases to 600 kHz ±6.25%

2.10.2 Power Enable/Power Good

The Mercury+ MP1 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters and LDOs for 1.05/1 V, 1.2 V, 1.8 V, 2.2 V and 2.5 V. The list of regulators that can be disabled via PWR_EN signal is provided in Section 2.10.1.

The PWR_EN input and PWR_GOOD signal are pulled to VCC_3V3 on the Mercury+ MP1 SoC module with a 4.7 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.10.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 14: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mercury+ MP1 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins (for example by connecting VCC_3V3 to VCC_IO directly) if PWR_EN is used to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 11.

2.10.3 Voltage Supply Inputs

Table 15 describes the power supply inputs on the Mercury+ MP1 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.8.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 13.2 V ±5%	Supply for the 1.05/1 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5 V voltage regulators. The 2.2 V supply is generated from the 2.5 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	1.8 - 5.5 V	Battery voltage for battery-backed RAM and battery-backed RTC

Table 15: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 16 presents the supply voltages generated on the Mercury+ MP1 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[2]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155 C-96, 103, 136, 143	3.3 V ±5%	1.5 A (and max 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89	2.5 V ±5%	0.5 A	Controlled by PWR_EN
VCC_1V8	B-52, 76, 108, 128 C-83, 123, 165	1.8 V ±5%	1 A	Controlled by PWR_EN

Table 16: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury+ MP1 SoC module.

2.10.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Microchip PolarFire and PolarFireSoc Power Estimator and Power Analyzer available on the Microchip website.

[2] The maximum available output current depends on your design. See sections 2.10.1 and 2.10.5 for details.

2.10.6 Heat Dissipation

High performance devices like the Microchip PolarFire SoC need cooling in most applications; always make sure the SoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury+ MP1 SoC module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the SoC device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on the board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 17 lists the heat sink and thermal pad part numbers that are compatible with the Mercury+ MP1 SoC module. Details on the Mercury heatsink kit can be found in the Mercury Heatsink Application Note [19].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury+ MP1	FCG1152 [22]	ACC-HS4-Set	ATS-52350G-C1-R0	TG-A6200-28-28-1

Table 17: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

Warning!

Depending on the user application, the Mercury+ MP1 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.10.7 Voltage Monitoring

Several pins on the module connector on the Mercury+ MP1 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 18 presents the VMON pins on the Mercury+ MP1 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V2	A-102	VCC_1V2	1.2 V on-board voltage
VMON_VTT	B-8	VCC_VTT	DDR termination voltage
VMON_VDD	B-168	VCC_VDD	Core voltage
VMON_2V5	B-167	VCC_2V5	2.5 V on-board voltage
VMON_1V8	C-8	VCC_1V8	1.8 V on-board voltage

Table 18: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.11 Clock Generation

A 50 MHz oscillator is used for the Mercury+ MP1 SoC module clock generation; the 50 MHz clock is fed to the HSIO bank 8 (pin AM5). A 125 MHz LVDS oscillator is connected to MSS.

A 24 MHz clock and a 25 MHz clock are used for the USB PHY and Ethernet PHYs respectively.
Table 19 describes the clock connections to the SoC device.

Signal Name	Frequency	Package Pin	SoC Pin Type
CLK50	50 MHz	AM5	HSIOPB8T4L6/CLKIN_N_12/CCC
MSS_REFCLK_P	125 MHz	V3	MSS_REFCLK_IN_P
MSS_REFCLK_N		W34	MSS_REFCLK_IN_N

Table 19: Module Clock Resources

2.12 Reset

There are three dedicated reset signals on the module; the device reset signal FPGA_DEVRST#, the peripheral reset signal RST_PER# and the MSS_RST# signal, which is the control signal of the peripheral reset.

Pulling FPGA_DEVRST# low resets the SoC device and the SPI Flash and additionally asserts RST_PER#. FPGA_DEVRST# is available on pin 132 of module connector pin A and has an on-board 4.7 kΩ pull-up resistor to VCC_CFG.

Pulling RST_PER# low resets the Ethernet PHY(s), the USB PHY, the QSPI and eMMC flash devices. RST_PER# can be asserted by pulling low MSS_RST# which is connected to the MSS of the SoC and has a 4.7 kΩ pull-up resistor to VCC_CFG.

Signal Name	Connector Pin	Package Pin	FPGA Pin Type	Description
FPGA_DEVRST#	A-132	G9	DEVRST_N	Device reset
RST_PER#	-	-	-	Peripheral reset
MSS_RST#	-	AA12	MSSIO12B4	Control signal of peripheral reset

Table 20: Reset Resources

Please note that FPGA_DEVRST# and RST_PER# are automatically asserted if PWR_GOOD is low.

2.13 LEDs

There are four active-low user LEDs on the Mercury+ MP1 SoC module - two of them are connected to the FPGA fabric only. The other two are connected to the FPGA fabric and the MSS. This results in 6 LED control signals. The LEDs will be on if at least one of its respective control signals is low.

Signal Name	Signal Location	LED Connection	Remarks
FPGA_LED0#	E23 (GPIO Bank 9)	LED 0	User function/active-low
MSS_LED0#	U14 (MSS Bank 2)	LED 0	User function/active-low
FPGA_LED1#	D23 (GPIO Bank 9)	LED 1	User function/active-low
MSS_LED1#	V12 (MSS Bank 2)	LED 1	User function/active-low
FPGA_LED2#	A25 (GPIO Bank 9)	LED 2	User function/active-low
FPGA_LED3#	B25 (GPIO Bank 9)	LED 3	User function/active-low

Table 21: User LEDs

2.14 DDR4 SDRAM (MSS)

There are two DDR4 SDRAM channels on the Mercury+ MP1 SoC module: one attached directly to the MSS side and one attached directly to the FPGA fabric.

The DDR4 SDRAM connected to the MSS is mapped to MSS Bank 6. The memory configuration on the Mercury+ MP1 SoC module supports ECC error detection and correction; the correction code type used is single bit error correction and double bit error detection (SEC-DED).

Three 16-bit memory chips are used to build an 36-bit wide memory (12 bits are unused): 32 bits for data and 4 bits for ECC.

The maximum memory bandwidth on the Mercury+ MP1 SoC module is:
1600 Mbit/sec × 32 bit = 6400 MB/sec

2.14.1 DDR4 SDRAM Characteristics

Table 22 describes the MSS memory availability and configuration on the Mercury+ MP1 SoC module.

Module	SDRAM Type	Density	Configuration	Manufact.
ME-MP1-D3EN (industrial)	AS4C512M16D4-75BIN	8 Gbit	512 M × 16 bit	Alliance Memory
ME-MP1-D4E (industrial)	H5ANAG6NCMR-XNI	16 Gbit	1 G × 16 bit	SK Hynix

Table 22: DDR4 SDRAM (MSS) Types

Warning!

Other DDR4 memory devices may be equipped in future revisions of the Mercury+ MP1 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.14.2 Signal Description

Please refer to the Mercury+ MP1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.14.3 Termination

Warning!

No external termination is implemented for the data signals on the Mercury+ MP1 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR4 SDRAM device.

2.14.4 Parameters

Please refer to the Mercury+ MP1 SoC module reference design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Libero project are presented in Table 23.

The values given in Table 23 are for reference only. Depending on the equipped memory device on the Mercury+ MP1 SoC module and on the DDR4 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR4
DRAM bus width	32 bit
ECC	Enabled
DRAM chip bus width	16 bits
DRAM chip capacity	8192 - 16384 Mbits
Bank group address width	1 - 2
Bank address width	2
Row address width	16
Column address width	10
Speed bin	DDR4-2666
Operating frequency	800 MHz
CAS latency	11
CAS write latency	11

Table 23: DDR4 SDRAM (MSS) Parameters

2.15 DDR4 SDRAM (FPGA Fabric)

The DDR4 SDRAM connected to the FPGA fabric is mapped to HSIO banks 0 and 8. The DDR bus width is 64-bit.

For standard speed grade rated SoC devices (MPFS250TS-FCG1152I) speeds up to 1333 Mbit/s (667 MHz) are supported by the memory controller and the equipped memory devices, whereas for -1 speed grade rated SoC devices (MPFS460TS-1FCG1152I) speeds up to 1600 Mbit/s (800 MHz) are supported by the memory controller and the equipped memory devices.

The maximum FPGA fabric memory bandwidth on the Mercury+ MP1 SoC module using -1 speed grade rated devices is:
1600 Mbit/sec × 64 bit = 12800 MB/sec

The maximum FPGA fabric memory bandwidth on the Mercury+ MP1 SoC module using STD speed grade rated devices is:
1333 Mbit/sec × 64 bit = 10664 MB/sec

2.15.1 DDR4 SDRAM Characteristics

Table 22 describes the memory availability and configuration on the Mercury+ MP1 SoC module.

Module	SDRAM Type	Density	Configuration	Manufact.
ME-MP1-D4E (industrial)	H5ANAG6NCMR-XNI	16 Gbit	1 G × 16 bit	SK Hynix

Table 24: DDR4 SDRAM (FPGA Fabric) Types

Warning!

Other DDR4 memory devices may be equipped in future revisions of the Mercury+ MP1 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

Please refer to the Mercury+ MP1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented for the data signals on the Mercury+ MP1 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR4 SDRAM device.

2.15.4 Parameters

Please refer to the Mercury+ MP1 SoC module reference design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Libero project are presented in Table 25.

The values given in Table 25 are for reference only. Depending on the equipped memory device on the Mercury+ MP1 SoC module and on the DDR4 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR4
DRAM bus width	64 bit
ECC	Disabled
DRAM chip bus width	16 bits
DRAM chip capacity	16384 Mbits
Bank group address width	2
Bank address width	2
Row address width	16
Column address width	10
Speed bin	DDR4-2666
Operating frequency	800 MHz
CAS latency	11
CAS write latency	11

Table 25: DDR4 SDRAM (FPGA Fabric) Parameters

2.16 QSPI Flash

The QSPI flash can be used to store application code and other user data.

2.16.1 QSPI Flash Characteristics

Table 26 describes the memory availability and configuration on the Mercury+ MP1 SoC module.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Infineon

Table 26: QSPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury+ MP1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.16.2 Signal Description

The QSPI flash is connected to MSS bank 2, pin MSSIO30 - MSSIO35.

The reset of the QSPI flash can be asserted by either MSS_RST# or FPGA_DEVRST#.

2.16.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, please refer to the flash device datasheet.

2.16.4 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the software needs to be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [27], [28].

2.17 SPI Flash

The SPI flash is intended for SPI master FPGA programming (Auto Update or In-Application Programming). Please refer to section 3.3 for details on programming the flash memory.

2.17.1 SPI Flash Characteristics

Table 27 describes the memory availability and configuration on the Mercury+ MP1 SoC module.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Infineon

Table 27: SPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury+ MP1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.17.2 Signal Description

The SPI flash can either be connected to the FPGA configuration pins on bank 3 or to the module connector pins via multiplexer controlled by the SRST# and SPI_FLASH_MODE signals (see section 3.3).

The reset of the SPI flash can be asserted by FPGA_DEVRST#.

2.18 eMMC Flash

The eMMC flash can be used for booting Linux and to store application code and other user data.

2.18.1 eMMC Flash Characteristics

The Mercury+ MP1 SoC module is equipped with a 16 GB eMMC flash.

Warning!

Different flash memory devices may be assembled depending on the revision of the Mercury+ MP1 SoC module. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.18.2 Signal Description

The eMMC flash signals are multiplxed with the SD card signals. If signal SDIO_SEL is set low, which is available on HSIO bank 8, the eMMC signals are routed to MSS bank 4 for 8 bit data transfer mode. The command signal has a 4.7 kΩ pull-up resistor to VCC_CFG and the data lines have 47 kΩ pull-up resistors to VCC_CFG.

2.18.3 Configuration

Following speed modes are supported, depending on VCC_CFG:
VCC_CFG = 3.3V: Default Speed (up to 26 MHz), High Speed (up to 52 MHz)
VCC_CFG = 2.5V: -
VCC_CFG = 1.8V: Default Speed (up to 26 MHz), High Speed (up to 52 MHz), HS200 (up to 200MHz)

2.19 SD Card

An SDIO interface is available on module connector A. This interface allows to attach an SD card via carrier board. Please note that external pull-up resistors are needed for SD card operation. For VCC_CFG = 1.8V, a level shifter to 3.3V is required (some level shifters also have built-in pull-ups). VCC_CFG = 2.5V is not supported in combination with SD card. For booting from an Ultra High Speed (UHS) SD card, an SD 3.0 compliant level shifter is required on the base board and VCC_CFG must be set to 1.8 V. Please note that this boot mode has not been tested, but it may be supported in the future.

The SD card can be used for booting Linux and to store application code and other user data. The SD card signals are multiplexed with the eMMC signals. The signal SDIO_SEL needs to be set high to configure the multiplexer for SD card operation. This configuration routes the SDIO signals on MSS bank 4 to the module connector A.

2.20 Dual Gigabit Ethernet

Up to two 10/100/1000 Mbps Ethernet PHYs are available on the Mercury+ MP1 SoC module. Both are connected via SGMII interfaces to the Microprocessor Subsystem.

2.20.1 Ethernet PHY Characteristics

Table 28 describes the equipped Ethernet PHY devices type on the Mercury+ MP1 SoC module.

PHY Type	Manufacturer	Type
DP83867IS	Texas Instruments	10/100/1000 Mbps

Table 28: Gigabit Ethernet PHYs Type

2.20.2 Signal Description

PHY 0 is connected to MSS Ethernet MAC 0 and PHY 1 is connected to MSS Ethernet MAC 1 through the dedicated SGMII pins at MSS bank 5.

The two Gigabit Ethernet PHYs have a shared MDIO interface and a shared interrupt line. The MDIO signals are connected to MSS bank 2, pin 28 and 29. These pins can be controlled by Ethernet MAC 1. The interrupt output of the Ethernet PHYs is connected to the I2C interrupt signal, available on MSS bank 4 pin 13.

The product models with one Ethernet PHY only have Ethernet PHY 1 equipped.

2.20.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.20.4 PHY Configuration

The configuration of the Ethernet PHYs is bootstrapped when the PHYs are released from reset. The bootstrap options of the Ethernet PHYs are set as indicated in Table 29.

Pin	Mode	Description
RX_D0	1 4	PHY0: MDIO address 0 PHY1: MDIO address 3
RX_D2	1 4	PHY0: MDIO address 0 PHY1: MDIO address 3
RX_CTRL	3	Enable autonegotiation
GPIO_1	1	Not relevant for SGMII operation
GPIO_0	1	Not relevant for SGMII operation
LED_2	1	Not relevant for SGMII operation
LED_1	1	Advertise 10/100/1000 ability
LED_0	2	Enable SGMII / disable MDI mirroring

Table 29: Gigabit Ethernet PHYs Configuration - Bootstraps

2.21 USB 2.0

One USB 2.0 PHY is available on the Mercury+ MP1 SoC module. Is connected to the MSS to I/O bank 2 and can be configured as device or host.

2.21.1 USB PHY Characteristics

Table 30 describes the equipped USB PHY device type on the Mercury+ MP1 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 30: USB 2.0 PHY Type

2.21.2 Signal Description

The ULPI interface for the PHY is connected to MSS pins 14-25 for use with the integrated OTG-compliant USB core.

2.22 Real-Time Clock (RTC)

The Mercury+ MP1 SoC module features a real-time clock. The RTC can be accessed by the I2C bus.

2.22.1 RTC Type

Table 31 describes the equipped RTC device type on the Mercury+ MP1 SoC module.

Device Type	Manufacturer	Type
ISL12020M	Renesas	Real-time clock

Table 31: Real-time clock Type

If the RTC functionality is needed, voltage VCC_BAT, which is located at pin A168 of module connector A, needs to be applied.

2.23 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.23.1 EEPROM Type

Table 32 describes the equipped EEPROM device type on the Mercury+ MP1 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
24AA128T-I/MNY (assembly option)	Microchip

Table 32: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mercury+ MP1 SoC module reference design [2].

2.24 Trusted Platform Module (TPM)

The Trusted Platform Module (TPM) is used to enhance the system security and enabling the implementation of a Trusted Computing Platform. Its functionalities include encryption, decryption, key management, signature functions, authentification, secured time and logging. Its SPI interface is connected to FPGA GPIO Bank 7.

2.24.1 TPM Type

Table 33 describes the equipped TPM device type on the Mercury+ MP1 SoC module.

Type	Manufacturer
SLI9670AQ20FW1311XUMA1	Infineon

Table 33: TPM Type

3 Device Configuration

3.1 Configuration Signals

Table 34 describes the most important configuration pins and their location on the module connector. These signals allow the user to program the SPI flash and SoC via SPI. Please refer to Section 3.7 for details.

Signal Name	SoC Pin Type	Mod. Conn. Pin	Description	Comments
FLASH_CLK	-	A-118	SoC SCK	4.7 kΩ pull-up to VCC_CFG Multiplexer to SoC. See section 3.3 for details
FLASH_DO	-	A-122	SoC SDO	Multiplexer to SoC. See section 3.3 for details
FLASH_DI	-	A-114	SoC SDI	4.7 kΩ pull-up to VCC_CFG Multiplexer to SoC. See section 3.3 for details
FLASH_CS#	-	A-116	SoC SS	4.7 kΩ pull-up to VCC_CFG Multiplexer to SoC. See section 3.3 for details
FPGA_DEVRST#	DEVRST_N	A-132	SoC device reset	4.7 kΩ pull-up to VCC_CFG
SRST#	HSIO	A-124	SPI Programming Mode Configuration Pin	4.7 kΩ pull-up to VCC_CFG Refer to section 3.3 for details
SPI_FLASH_MODE	IO_CFG_INTF HSIO	A-126	SPI Programming Mode Configuration Pin	4.7 kΩ pull-up to VCC_CFG
SDIO_SEL	HSIO	-	Select SDIO or eMMC	SDIO or eMMC interface selection. 4.7 kΩ pull-up to VCC_3V3_SEQ

Table 34: SoC Configuration Pins

3.2 Module Connector C Detection

Signal C_PRSNT# (pin C-167) must be connected to GND on the base board if the designed base board has three connectors. Depending on the value of this pin, the FPGA banks routed to module connector C are supplied with the voltages provided by the user (when C_PRSNT# is low) or with a default voltage of 3.3 V (when C_PRSNT# is unconnected).

C_PRSNT# is equipped with a 4.7 kΩ pull-up resistor on the module.

3.3 SPI Programming Modes

There are three PolarFire SoC programming modes. Two of these three modes are via the SPI interface of the SoC (referred as PF Bank 3 in table 35), which are described in this section. The other one is through the JTAG interface. For more information on the JTAG programming mode please refer to section 3.4.

For SPI configuration modes the SoC can either act as the slave or master. On the Mercury+ MP1 SoC module a third SPI programming mode can be configured, giving the user access to the SPI flash mermory by a external master and bypassing the SoC.

Table 35 gives an overview over these three SPI programming mode configuration options which can be set via the two configuration signals SPI_FLASH_MODE and SRST#.

SPI_FLASH_MODE	SRST#	SPI Master	SPI Slave	Bitstream Source
0	0	Carrier	SPI Flash	FPGA
0	1	Carrier	PF Bank 3	FPGA
1	X	PF Bank 3	SPI Flash	FPGA/SPI-Flash

Table 35: SPI Programming Mode Configuration Options

For more details on Microchip PolarFire SoC programming please refer to the PolarFire® FPGA and PolarFire SoC FPGA Programming User Guide [26].

3.4 JTAG

PolarFire devices include a JTAG controller which is able to communicate with the PolarFire system controller and can be used for programming, system testing, debugging.

3.4.1 JTAG on Module Connector

The module connector locations of the JTAG interface are given in 36.

Signal Name	Module Connector Pin	PolarFire Pin	Resistor
JTAG_TCK	A-123	TCK	4.7 kΩ pull-down to GND
JTAG_TMS	A-119	TMS	4.7 kΩ pull-up to VCC_CFG
JTAG_TDI	A-117	TDI	4.7 kΩ pull-up to VCC_CFG
JTAG_TDO	A-121	TDO	-

Table 36: JTAG Interface

3.4.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VJTAG pin of the programmer must be connected to VCC_CFG.

It is recommended to add a 22 Ω series termination resistor on the TCK signal and 100 Ω series termination resistors on the other signals between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

Warning!

On Enclustra base boards, the pin assignment of the JTAG connector is different than the Microchip FlashPro Programmer. An adapter needs to be used to interface with the Microchip FlashPro Programmer.

3.4.3 JTAG Programming Mode

The PolarFire SoC can be programmed via the JTAG interface. In JTAG programming mode, the SoC can be programmed by the use of a FlashPro Programmer or an external Microprocessor. For details please refer to the PolarFire® FPGA and PolarFire SoC FPGA Programming User Guide [26].

3.5 eMMC Flash Programming

The USB service in Hart Software Services (HSS) software can be used to program the eMMC memory. With the USB PHY equipped on the module configured in device mode, the eMMC (or SD card) can be used as USB flash drive. This service allows to format and partition the eMMC by any host computer.

See Microchip documentation or the Linux reference design documentation [16] for more details.

3.6 SPI Flash Programming via JTAG

The Microchip Libero SoC Design Suite software offers SPI flash programming support via JTAG.

3.7 SPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the PS_SRST# signal to GND followed by a pulse on PS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Figure 12 shows the signal diagrams corresponding to flash programming from an external master.

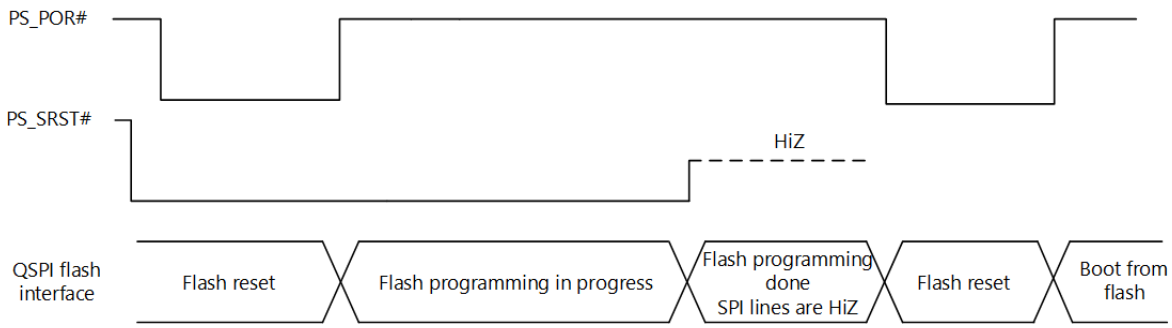

Figure 12: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mercury+ MP1 SoC module.

3.8 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using Enclustra Module Configuration Tool (MCT) [18]. The Mercury+ MP1 SoC moduleis supported starting with version 2.10. The entire procedure is described in the reference design documentation.

The internal flash of the Mercury+ MP1 SoC moduleis available to be programmed trought the SPI bus, but currently cannot be programmed with the MCT. The MCT, however, can be used to erase the contents of the internal flash starting with MCT version 2.10. Due to limitations of the ST1 baseboard, the SPI communication from MCT to SoC is one-way only and procedures using the SPI bus are not available.

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury+ MP1 SoC module is connected to the SoC device, the EEPROM, to the DC/DC power converters, to the RTC and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 37 describes the signals of the I2C interface - the pins are connected to both MSS and FPGA fabric. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an open drain signal, has a pull-up resistor to VCC_CFG and must not be driven high by the SoC.

Level shifters are used between the I2C bus and SoC pins, as MSS bank 2, MSS bank 4 and FPGA GPIO bank 1 are supplied with different voltages. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	MSS Pin	Package Pin	Connector Pin	Resistor
I2C_SDA	MSSIO27	V13	A-113	2.2 kΩ pull-up
I2C_SCL	MSSIO26	V14	A-111	2.2 kΩ pull-up
I2C_INT#	MSSIO13	Y12	A-115	4.7 kΩ pull-up

Table 37: I2C Signal Description

4.3 I2C Address Map

Table 38 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x54	Secure EEPROM (assembly option, refer to Section 2.23)
0x57	RTC user SRAM
0x6F	RTC registers
0x11	Power Converter
0x17	Power Converter

Table 38: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read data from the EEPROM is included in the Mercury+ MP1 SoC module Linux BSP.

Warning!
The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 39: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury+ MP1 SoC module	0x0339	0x[XX]	0x[YY]	0x0339 [XX][YY]

Table 40: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC type	0	2	See SoC type table (Table 42)
	3-0	SoC device speed grade	0	1	See SoC type table (Table 43)
0x09	7-6	Temperature range	0	2	See temperature range table (Table 44)
	5	Reserved	-	-	
	4-3	Gigabit Ethernet port count	0	2	
	2-0	Reserved	-	-	
0x0A	7-4	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1
	3-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR4 ECC RAM (MSS) size (GB)	0 (0 GB)	3 (4 GB)	Resolution = 1 GB
	3-0	DDR4 RAM (FPGA fabric) size (GB)	0 (0 GB)	4 (8 GB)	Resolution = 1 GB
0x0C	7-4	QSPI MSS flash size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
	3-0	SPI FPGA flash size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB

Table 41: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 1 GB, DRAM=2: 2 GB, DRAM=3: 4 GB, etc).

Table 42 shows the available SoC types.

Value	SoC Device Type
0	MPFS250T ES
1	MPFS250TS
2	MPFS460TS

Table 42: SoC Device Types

Table 43 shows the available speed grade.

Value	Module Speed Grade
0	-1
1	Standard

Table 43: Module Speed Grade

Table 44 shows the available temperature ranges.

Value	Module Temperature Range
0	Industrial
1	Extended
2	Engineering Sample

Table 44: Module Temperature Range

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 45 indicates the absolute maximum ratings for Mercury+ MP1 SoC module.

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.3 to 16	V
VCC_BAT	Supply voltage for battery-backed RAM and battery-backed RTC	-0.3 to 6	V
VCC_IO_B1 VCC_IO_B7 VCC_IO_B9 VCC_CFG	Power supply for IO banks	-0.3 to 3.6	V
V_IO	GPIO input voltage relative to GND	-0.5 to 3.8	V
Temperature	Temperature range for extended temperature modules (E)*	0 to +85	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 45: Absolute Maximum Ratings

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

5.2 Recommended Operating Conditions

Table 46 indicates the recommended operating conditions for Mercury+ MP1 SoC module.

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 13.86	V
VCC_BAT	Supply voltage for battery-backed RAM and battery-backed RTC	1.8 to 5.5	V
VCC_IO_B1 VCC_IO_B7 VCC_IO_B9 VCC_CFG	Power supply for IO banks relative to GND	Refer to section 2.8.5	V
V_IO	I/O input voltage relative to GND	0 to VDDI	V
Temperature	Temperature range for extended temperature modules (E)* Temperature range for industrial modules (I)*	0 to +85 -40 to +85	°C °C

Table 46: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

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