Mercury+ ST1 Base Board

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ ST1 base board to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ ST1 base board.

Summary

This document first gives an overview of the Mercury+ ST1 base board followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-ST1	Mercury+ ST1 Base Board

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-456-001	03	16.02.2021

Approval Information	Name	Position	Date
Written by	HMEY, NALI	Design Engineer	07.05.2020
Verified by	HMEY	Design Expert	11.05.2020
Approved by	DIUN	Manager, BU SP	16.02.2021

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Document History

Version	Date	Author	Comment
03	16.02.2021	DIUN	Added information on Altium design files, updated USB annex to clarify better the use cases, other style updates.
02	23.07.2020	HMEY	Added information on the MIPI interfaces, added product pictures and weight, other minor corrections and additions.
01	09.06.2020	HMEY	Version 01, preliminary

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ ST1 base board is equipped with a multitude of I/O connectors for use with Mercury family FPGA and SoC modules. The board is well-suited for rapid prototyping and for building FPGA systems, without the need for developing custom hardware.

The board can also be used for production flash programming on Mercury modules, or for educational purposes.

This board is specially designed for image processing applications.

The main features of the Mercury+ ST1 base board are:

- Support for USB 3.0 host and USB 3.0 device
- FTDI USB 2.0 High-Speed device controller
- High-speed FPGA and flash programming over USB
- FMC HPC Connector
- Versatile set of I/O connectivity options
- 2 × Ethernet RJ45 connectors
- SFP+ connector
- 2 × MIPI D-PHY interfaces (CSI , CSI/DSI)
- HDMI 2.0a connector
- Mini DisplayPort connector
- Low-jitter clock generator
- microSD card slot
- Simple integration by using a single 12 V voltage supply
- Small solution size

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

1.1.3 RoHS

The Mercury+ ST1 base board is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury+ ST1 base board must be properly disposed of at the end of its life. If a battery is installed on the board, it must also be properly disposed of.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ ST1 base board.

1.1.5 Safety Recommendations and Warnings

Mercury boards are not designed to be “ready for operation” for the end-user. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing a Mercury module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the board and to the equipped module.

Warning!

It is possible to mount some Mercury modules the wrong way round on the Mercury+ ST1 base board - always check that the mounting holes on the base board are aligned with the mounting holes of the module.

Every Mercury module has a 1 mm copper square module marker, which has its counter part on the base board. If these module markers are aligned, proper orientation is granted. The copper square can be found in a corner of the module, on top as well as on the bottom side.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

Warning!

Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

Always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ ST1 base board. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ ST1 base board is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Deliverables

- Mercury+ ST1 base board including plastic standoffs
- Mercury+ ST1 base board documentation, available via download:
  - Mercury+ ST1 Base Board User Manual (this document)
  - Mercury+ ST1 Base Board IO Net Length Excel Sheet [3]
  - Mercury+ ST1 Base Board User Schematics (PDF) [4]
  - Mercury+ ST1 Base Board Known Issues and Changes [5]
  - Mercury+ ST1 Base Board 3D Model (PDF) [6]
  - Mercury+ ST1 Base Board STEP 3D Model [7]
  - Mercury Mars Module Pin Connection Guidelines [8]
  - Mercury Master Pinout [9]

1.3 Accessories

- Mercury FPGA or SoC module
- 12 V DC/1.5 A power supply
- USB 2.0 A to micro-B USB cable

1.4 Design Files

The Altium design files for the Mercury+ ST1 base board are available upon request after signing a design license agreement. Please contact Enclustra for further information.

2 Getting Started

This section contains essential information on using the Mercury+ ST1 base board.

Before first use of the Mercury+ ST1 base board with a Mercury or Mercury+ module, the following steps must be followed:

- Mount the module on the module slot on the base board, with the power switched off.

Warning!

It is possible to mount some Mercury modules the wrong way round on the Mercury+ ST1 base board - always check that the mounting holes on the base board are aligned with the mounting holes of the module.

Every Mercury module has a 1 mm copper square module marker, which has its counter part on the base board. If these module markers are aligned, proper orientation is granted. The copper square can be found in a corner of the module, on top as well as on the bottom side.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

Warning!

Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

Always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ ST1 base board. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

- Set the DIP switches correctly (refer to Section 6.3).
- Set the I/O voltage selection jumpers correctly (refer to Section 5.6).
- Power up the board (refer to Section 5 for power options).

The power supply of the base board must be turned off in the following situations:

- Before changing the position of the I/O voltage selection jumpers
- Before removing the Mercury or Mercury+ module
- Before connecting or disconnecting peripherals to ANIOS and I/O connectors
- Before connecting or disconnecting FMC cards

Before connecting peripherals, make sure that the corresponding VCC_IO voltage is properly set.

The operating conditions for the Mercury+ ST1 base board and equipped module must conform to the values given in Section 7, and in the relevant section from the Mercury or Mercury+ module user manual.

Warning!

The Mercury+ ST1 base board can only be used in combination with a Mercury or Mercury+ module. When using the board without module the "PWGD" LED will remain off; refer to Section 6.1 for details.

3 Board Description

3.1 Block Diagram

The Mercury+ ST1 base board can be used in combination with any Mercury module. Depending on the equipped module some features may not be available.

The block diagram of the Mercury+ ST1 base board is shown in Figure 1.

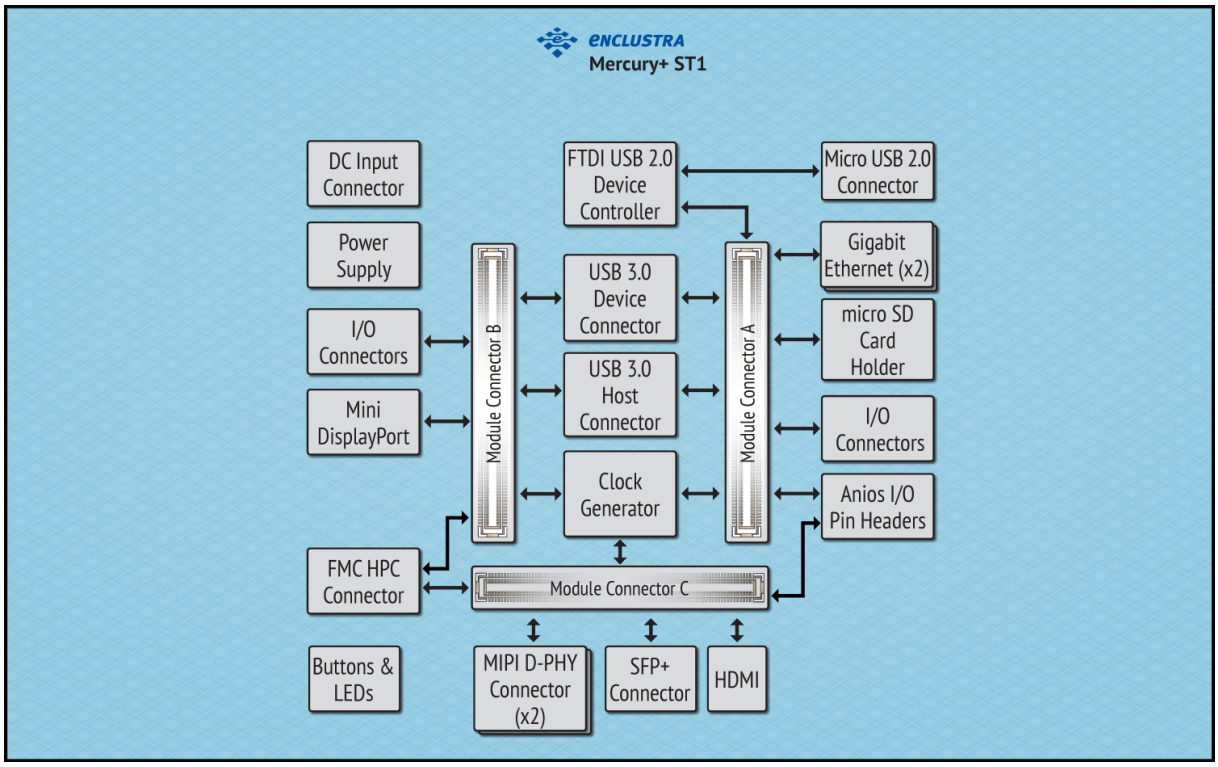


Figure 1: Hardware Block Diagram

3.2 Features

Table 1 describes the features available on the Mercury+ ST1 base board.

Feature	Description
Form factor	120 × 100 mm
System features	Built-in Xilinx JTAG (via USB connection) Low-jitter clock generator Programmable user oscillator (optional)
Memory	microSD card holder
Connectors	2 × USB 3.0 connectors (host & device) 2 × RJ45 Gigabit Ethernet connectors Micro USB (FTDI USB 2.0 High-Speed device controller) Mini DisplayPort connector SFP+ connector FMC HPC connector 2 × MIPI D-PHY connectors (CSI , CSI/DSI) HDMI 2.0 connector
User I/Os	2 × 40-pin Anios pin headers 3 × 12-pin IO connectors 2 × user push bottons
Supply voltage	12 V DC (internal, external)

Table 1: Base Board Features

Warning!
Please note that the available features depend on the equipped Mercury FPGA/SoC module.

3.3 Board Configuration and Product Codes

Table 2 describes the standard base board configuration. Custom configurations are available; please contact Enclustra for further information.

Product Code	Features	Temperature Range
ME-ST1-W	Refer to Table 1	-20..+75° C

Table 2: Standard Base Board Configuration

3.4 Article Numbers and Article Codes

Every board is uniquely labeled, showing the article number and serial number. An example is presented in Figure 2.

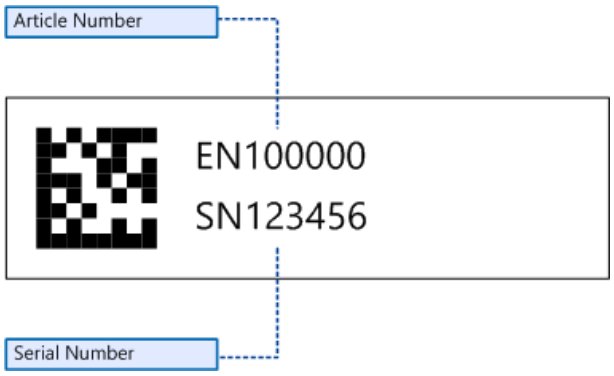


Figure 2: Product Label

The correspondence between article number and article code is shown in Table 3. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury+ ST1 Base Board Known Issues and Changes document [5].

Article Number	Article Code
EN102868	MA-ST1-W-R1

Table 3: Article Numbers and Article Codes

3.5 Top and Bottom Views

3.5.1 Top View

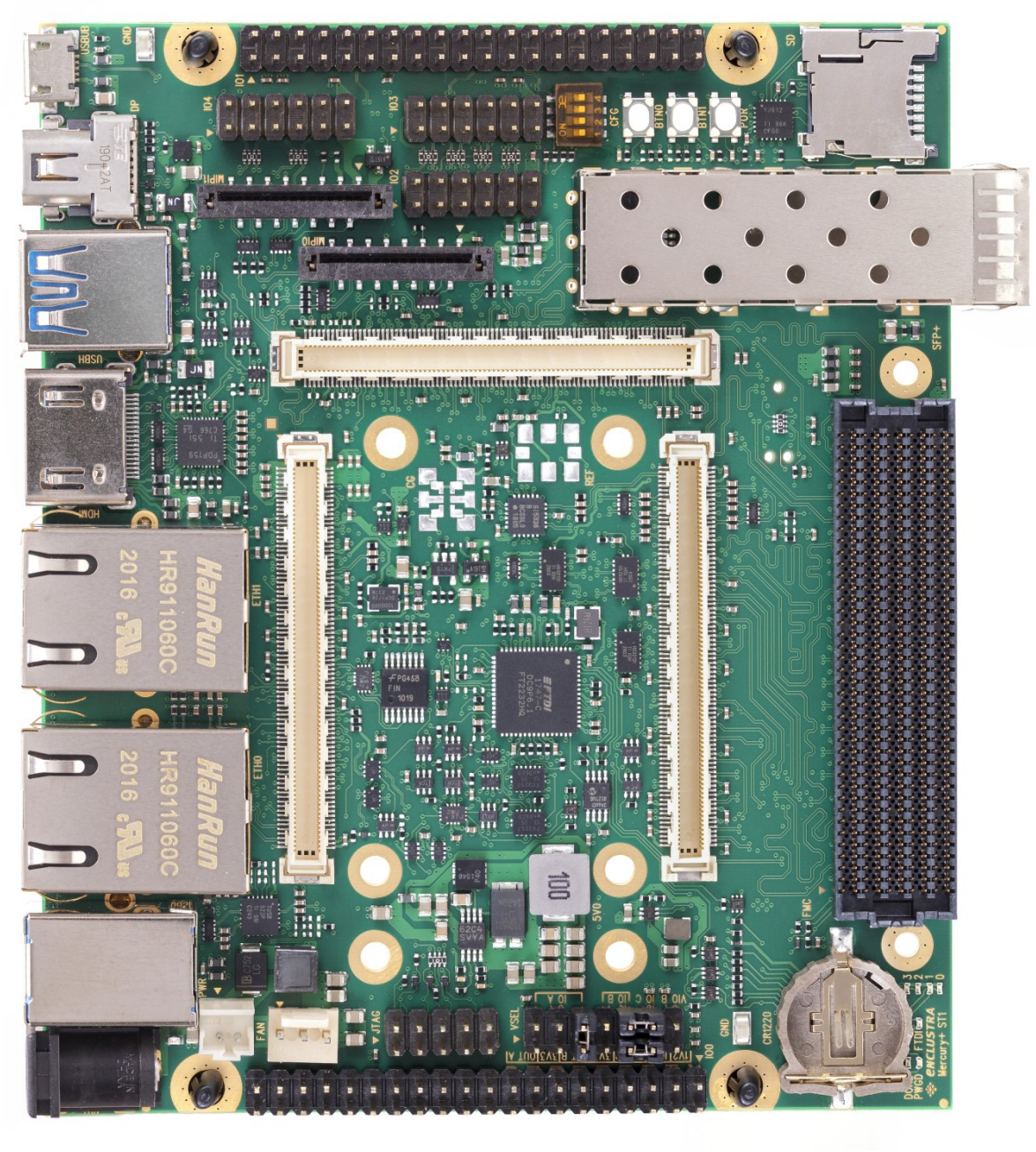


Figure 3: Board Top View

3.5.2 Bottom View

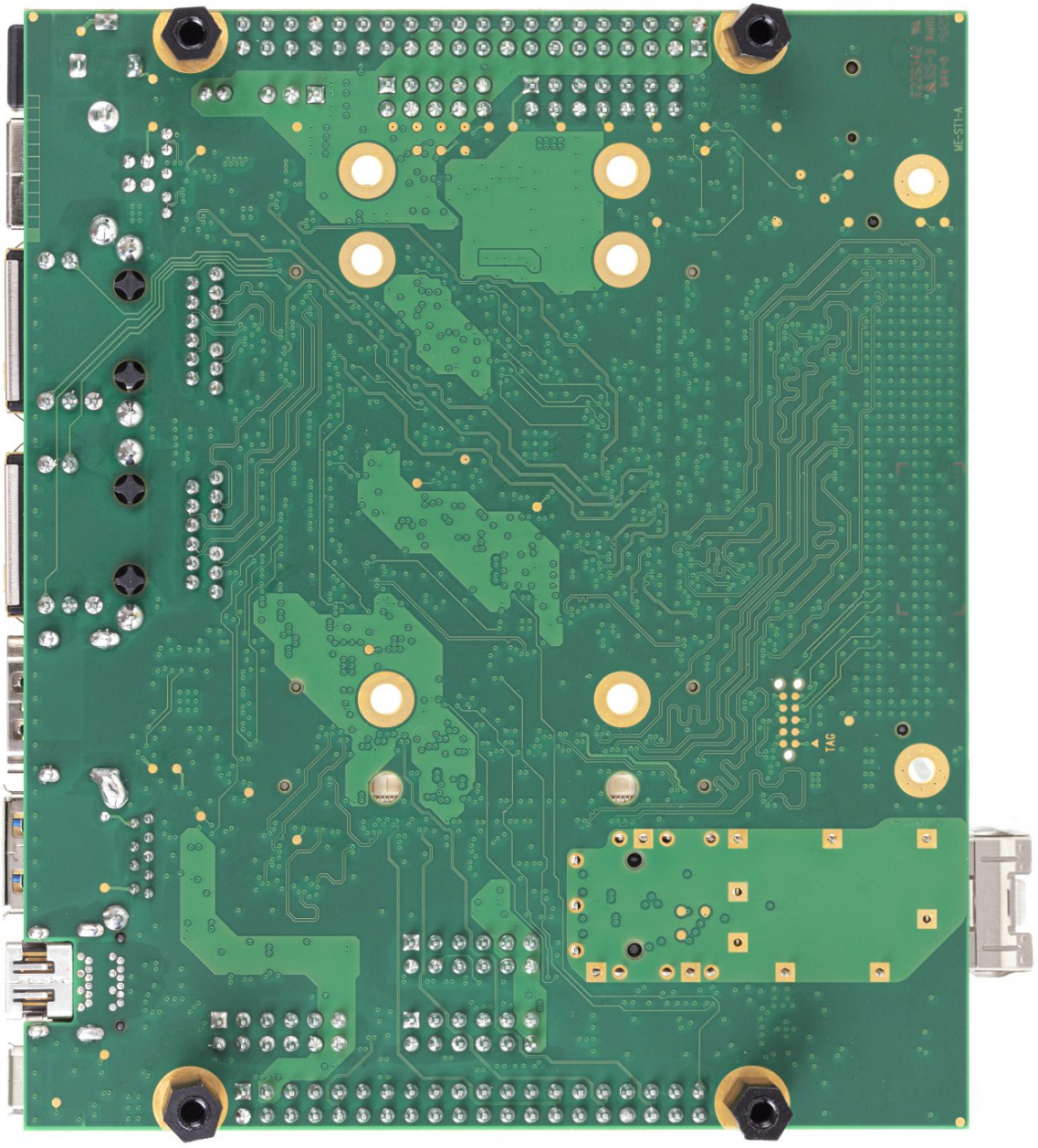


Figure 4: Board Bottom View

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.6 Top and Bottom Assembly Drawings

3.6.1 Top Assembly Drawing

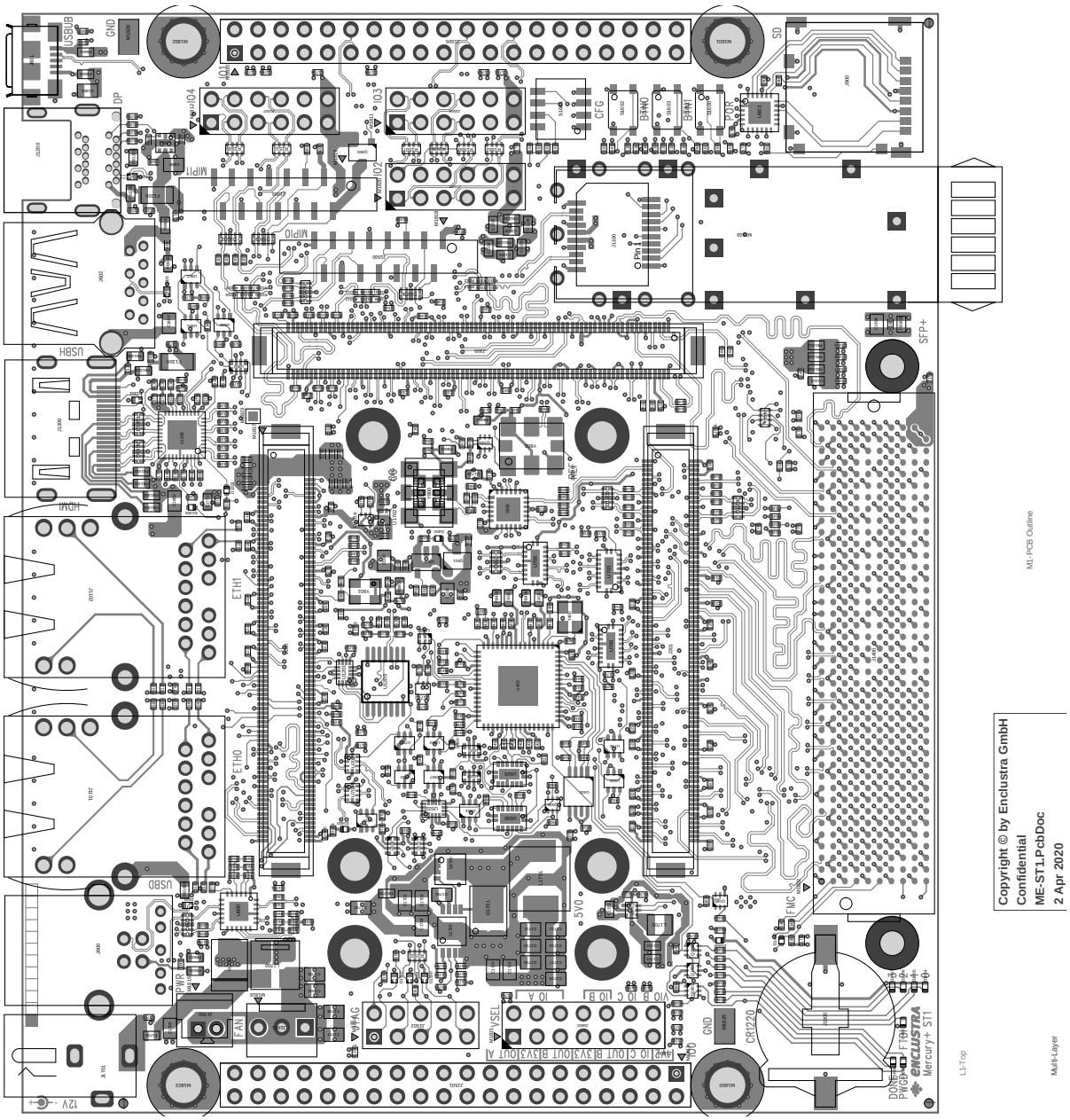


Figure 5: Board Top Assembly Drawing

3.6.2 Bottom Assembly Drawing

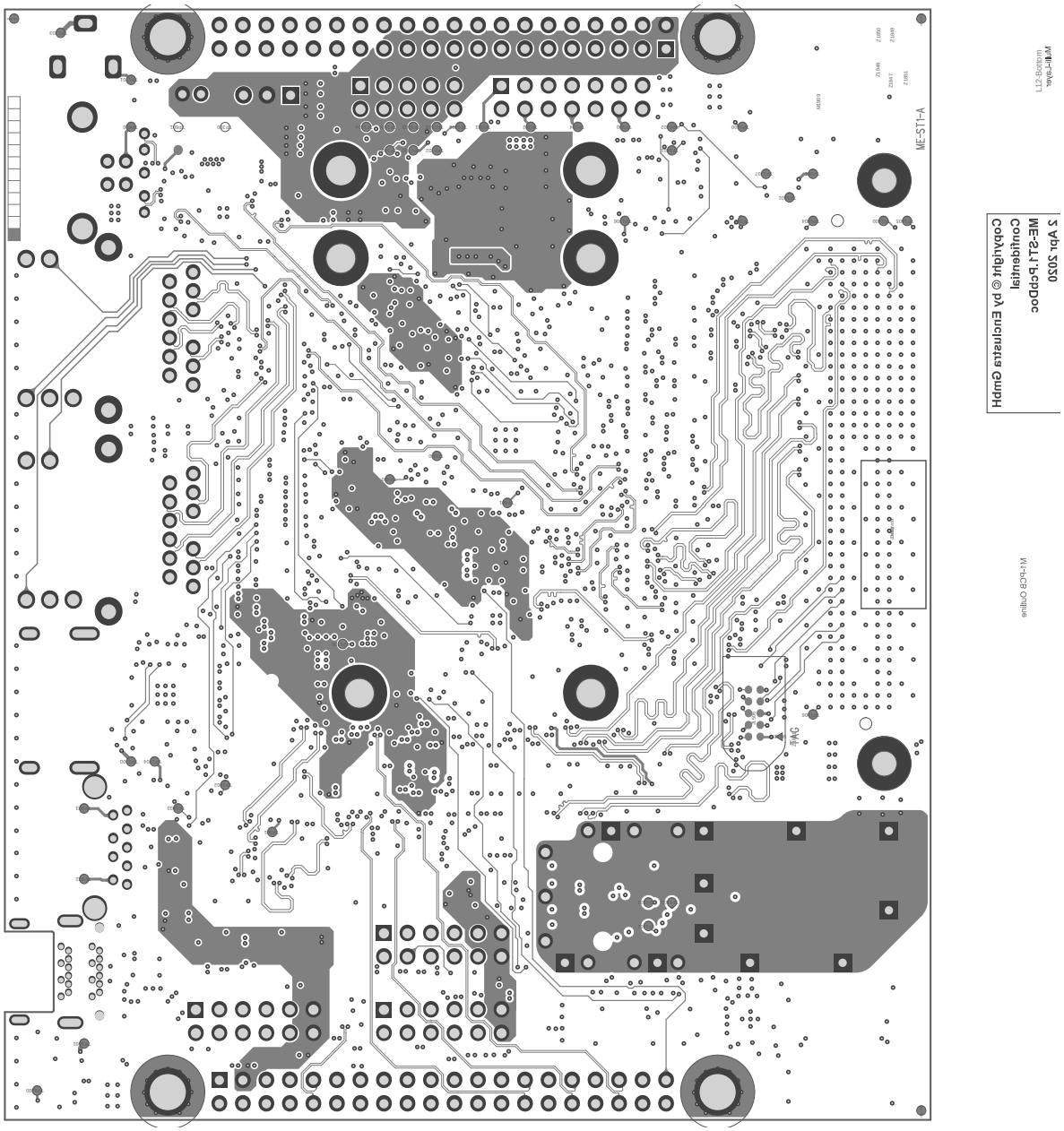


Figure 6: Board Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.7 Board Dimensions

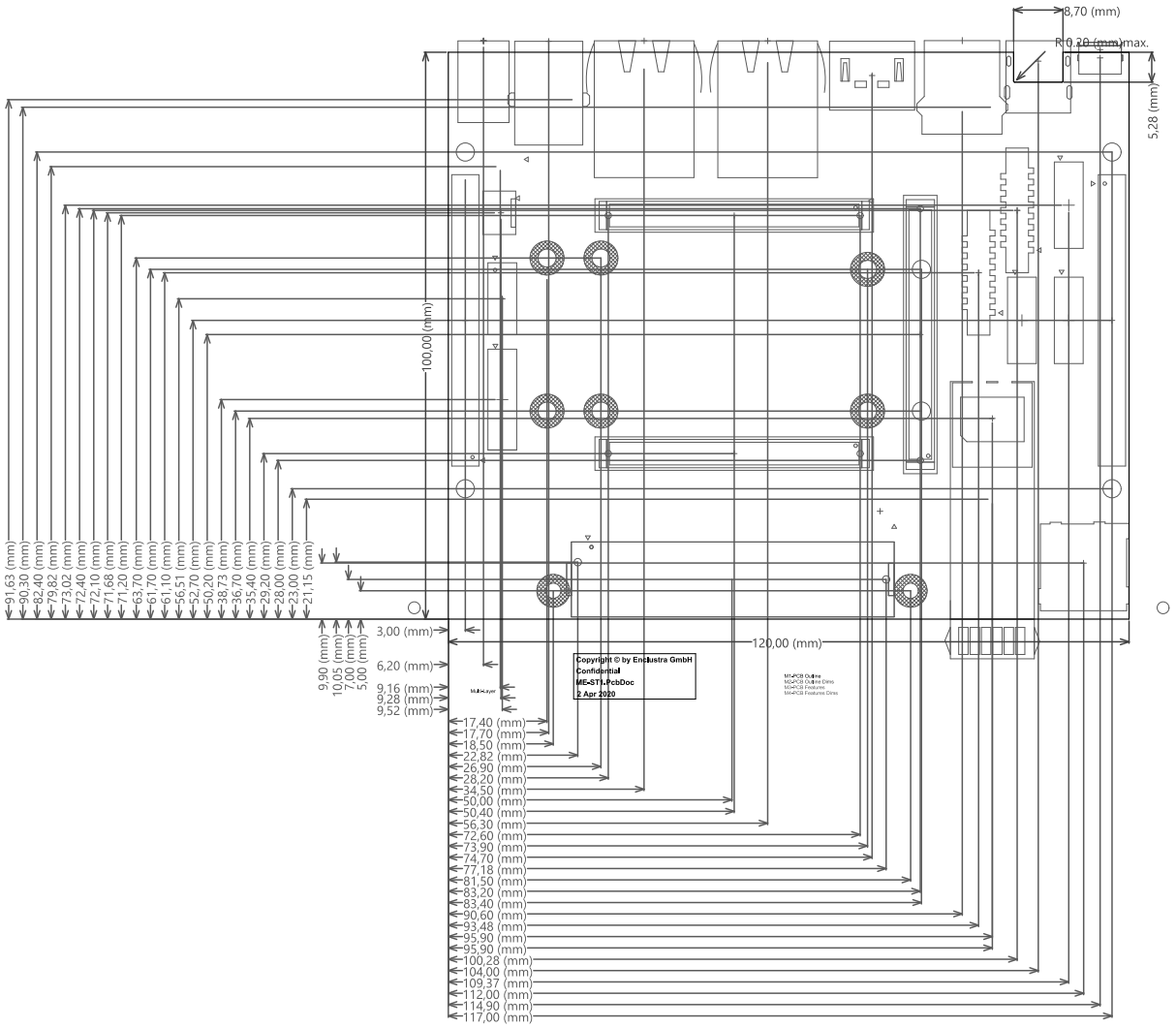


Figure 7: Board Dimensions

3.8 Mechanical Data

Table 4 describes the mechanical characteristics of the Mercury+ ST1 base board. A 3D model (PDF) and a STEP 3D model are available [6], [7].

Symbol	Value
Size	120 × 100 mm
Component height top	11.3 mm
Component height bottom	8 mm plastic standoffs equipped on bottom side
Weight	100 g (without battery and module)

Table 4: Mechanical Data

3.9 Mechanical Components

Table 5 describes the mechanical components present on the Mercury+ ST1 base board. The listed elements are for reference only. Any other components that meet the requirements may be used.

Product Number	Manufacturer	Description
973080365	Würth Elektronik	4 × plastic spacer bolt with female thread/clip, length 8 mm

Table 5: List of Mechanical Components

4 Connectors Description

4.1 12 V External Power (J1701)

This connector is used to supply the main VCC input voltage.

Apply only 12 V DC to this connector.

Pin Number	Signal Name	Description
1 (inner)	VCC_MAIN_IN	12 V DC (nominal) input voltage
2 (outer)	GND	Ground

Table 6: J1701 - External Power Connector

Type	Manufacturer
PJ-102AH	CUI

Table 7: J1701 - External Power Connector Type

4.2 12 V Internal Power (J1700)

The Mercury+ ST1 base board base board can alternatively be powered through the internal power input connector J1700. The 12 V DC power source connected to J1700 must be filtered by external power circuitry.

Apply only 12 V DC to this connector.

Pin Number	Signal Name	Description
1	VCC_MAIN	12 V DC (nominal) input voltage
2	GND	Ground

Table 8: J1700 - Internal Power Connector

Type	Manufacturer
292132-2	TE Connectivity

Table 9: J1700 - Internal Power Connector Type

Warning!
Do not short circuit the 12 V power supply, and make sure the currents flowing through the pins of this connector do not exceed 2.0 A. Otherwise, the PCB may be damaged.

4.3 Fan Connector (J1601)

An external 12 V fan can be connected to J1601 connector.

Pin Number	Signal Name	Description
1	GND	Ground
2	VCC_MAIN	12 V DC (nominal) input voltage
3	NC	-

Table 10: J1601 - Fan Connector

Type	Manufacturer
61900311121	Würth Elektronik

Table 11: J1601 - Fan Connector Type

Table 12 shows an example of a mating part for the fan connector. This connector is without female crimp contacts or wires.

Type	Manufacturer
61900311621	Würth Elektronik

Table 12: Mating Part for the Fan Connector

4.4 I/O Voltage Selection (J1602)

The I/O voltage selection jumpers are used to configure the VCC_IO_A, VCC_IO_B and VCC_IO_C voltages that power the I/O banks of the SoC/FPGA device on the Mercury module. Refer to Section 5.6 for details.

4.5 Mercury Module Connector (J200/J201/J300)

A detailed pinout of the Mercury module connector can be found in the Mercury Master Pinout [9] and in the Mercury+ ST1 Base Board User Schematics [4].

Warning!

Only Enclustra Mercury FPGA/SoC modules should be inserted into the Mercury+ ST1 base board.

Warning!

The VCC_IO pins are directly connected to the FPGA/SoC device. Apply only compliant voltages to the VCC_IO pins; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ ST1 base board.

4.6 USB 3.0 Host Connector (J602)

The Mercury+ ST1 base board is equipped with a type-A USB 3.0 host connector.

If the mounted Mercury module features a USB controller, the module's USB signals can be connected to J602 via a multiplexer. Details on USB connections on the board are available in Section 6.5.

The power and data signals on this connector are ESD-protected.

4.7 USB 3.0 Device Connector (J600)

The Mercury+ ST1 base board is equipped with a type-B USB 3.0 device connector.

If the mounted Mercury module features a USB controller, the module's USB signals can be connected to J600 via a multiplexer. Details on USB connections on the board are available in Section 6.5.

The power and data signals on this connector are ESD-protected.

4.8 Micro USB 2.0 Device Connector (J601)

The micro USB connector on the board is connected to the FTDI device. It can be used for UART, SPI and I2C communication. Refer to Section 6.5.2 for details on the FTDI device.

4.9 Gigabit Ethernet Ports (J1101/J1102)

The Mercury+ ST1 base board is equipped with two 10/100/1000 Mbit Ethernet ports. The capability of the Ethernet interface depends on the connected Mercury module.

The RJ45 connectors are connected through magnetics directly to the Mercury module connector. For details on the Ethernet interface, refer to Section 6.4.

4.10 SFP+ Connector (J1100)

The Mercury+ ST1 base board is equipped with a SFP+ socket. The capability of the SFP+ interface depends on the connected Mercury module as well as on the plugged SFP+ module.

The SFP+ connector J1100 is connected by default to the Mercury module connector C, pins C-63/65 (TX side) and C-66/68 (RX side).

4.11 MIPI Connectors (J1000/J1001)

The Mercury+ ST1 base board is equipped with two MIPI connectors, each with 2 signal lanes. The signals available on these connectors are routed to/from the FPGA banks on the SoC/FPGA device on the Mercury module. Refer to section 6.9 for details on connectivity options.

The pinout on the J1000 and J1001 connectors corresponds to the Raspberry Pi pinout. In order to receive and transmit video signals through the links, FPGA support is required (video protocol implementation).

The signals on the connectors are ESD-protected.

4.12 HDMI Connector (J1300)

The Mercury+ ST1 base board is equipped with an HDMI connector. The signals available on this connector are routed to/from the FPGA banks on the SoC/FPGA device on the Mercury module via HDMI Redriver U1300. Refer to section 6.7 for details on the HDMI interface and connectivity options.

The signals on this connector are ESD-protected.

The pinout on the J1300 connectors corresponds to the HDMI standard. In order to transmit video signals through the links, FPGA support is required (video protocol implementation).

4.13 Mini DisplayPort Connector (J1200)

The Mercury+ ST1 base board is equipped with a Mini DisplayPort connector. The signals available on this connector are routed to/from the FPGA banks on the SoC/FPGA device on the Mercury module. Refer to section 6.8 for details on the DisplayPort interface.

The signals on this connector are ESD-protected.

The pinout on the J1200 connectors corresponds to the Mini DisplayPort standard. In order to receive and transmit video signals through the links, FPGA support is required (video protocol implementation).

4.14 microSD Card Slot (J900)

The enclosure of J900 is connected to GND.

The microSD card signals are connected via a multiplexer with a built-in level shifter to the Mercury module SDIO signals.

4.15 FMC Connector (J1400)

This connector allows the extension of the Mercury+ ST1 base board with other FMC (FPGA Mezzanine Card) modules (Enclustra or third-party).

For details on the pinout of the FMC LPC (Low Pin Count) and HPC (High Pin Count), please refer to the VITA 57 FMC specification.

Table 13 describes the FMC connector present on the Mercury+ ST1 base board.

Warning!

The FMC I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ ST1 base board.

Board Variant	FMC Connector Name	Connector Type	Manufacturer
ME-ST1-W	FMC HPC connector	ASP-134486-01	Samtec

Table 13: J1400 - FMC HPC Connector Type

Table 14 includes information related to the total number of I/Os available on the FMC connector.

Note that certain user-defined I/Os or multi-gigabit transceivers and clocks are supported only in combination with Mercury+ modules, which are equipped with a third connector (module connector C).

Signal Name	FMC Pin Type	Single Ended	Pairs	Module Connector
FMC_LA<0-1>_CC_P/N	LA CC	4	2	B
FMC_LA<17-18>_CC_P/N	LA CC	4	2	B
FMC_LA<2-16>_P/N	LA	30	15	B
FMC_LA<19-33>_P/N	LA	30	15	B
FMC_HA<0-1>_CC_P/N	HA CC	4	2	C
FMC_HA<2-17>_P/N	HA	32	16	C
FMC_CLK<0-1>_M2C_P/N	CLK M2C	-	2	B
FMC_DP<0-3>_C2M_P/N	DP C2M	-	4	B
FMC_DP<4-7>_C2M_P/N	DP C2M	-	4	C
FMC_DP<0-3>_M2C_P/N	DP M2C	-	4	B
FMC_DP<4-7>_M2C_P/N	DP M2C	-	4	C
FMC_GCLK0_M2C_P/N	GBTCLK M2C	-	1	B
FMC_GCLK1_M2C_P/N	GBTCLK M2C	-	1	C

Table 14: Available I/Os on the FMC Connector

The signal names on the module connectors indicate to which pins of the FMC HPC connector they are routed to. Please note that although HA17 is usually a CC (clock-capable) pin in the FMC standard, it has not been routed to a clock-capable pin on the Mercury connector, therefore the signal name does not contain the "CC" part.

Both GBT M2C clock pairs are AC coupled. The user-defined signals on bank B located on the HPC (HB signals) are not interfaced to Mercury module connectors and therefore not supported.

The FMC I2C interface is connected to the FPGA I2C interface (I2C_SDA/SCL_FPGA) available on module connector A.

Please refer to the Mercury Master Pinout [9] and the Mercury+ ST1 Base Board User Schematics [4], for details on FMC connectivity.

4.16 FMC JTAG Connector (J1506)

The FMC JTAG connector allows accessing the JTAG port of the mounted FMC. The signals on this connector can be accessed with a TC2050-IDC-NL plug of nails, in combination with a TC2050-CLIP.

To ensure a high data throughput, this JTAG connectivity is not chained to the Mercury module. Series termination resistors are equipped between the module signals and the JTAG header.

The TAG plug of nails connector is not equipped by default on Mercury+ ST1 base board.

Pin Number	Connection	Series Resistor
1	VCC_3V3_MOD	-
2	FMC_TMS	100 Ω
3, 5, 7, 9	GND	-
4	FMC_TCK	22 Ω
6	FMC_TDO	100 Ω
8	FMC_TDI	100 Ω
10	FMC_TRST#	100 Ω

Table 15: J1506 - FPGA TAG Connector

Warning!

The JTAG pins are connected to the FMC Mezzanine device via small-value series resistors. Use only VCC_IO voltages compliant with the equipped FMC Mezzanine device. Any other voltages may damage the equipped FMC Mezzanine device.

4.17 Anios I/O Connector IO0/IO1 (J1501/J1505)

The Anios I/O connectors can be used for user applications: each connector provides 24 user I/Os, a differential clock connection, connectivity to the I2C bus, and power supply connections. The clock, data and I2C signals are routed to the module connector - for details, refer to the Mercury+ ST1 Base Board User Schematics [4].

Warning!

The Anios I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ ST1 base board.

4.18 I/O Connectors IO2/IO3/IO4 (J1500/J1504/J1507)

Three I/O connectors (2 x 6) male pin headers can be used for user applications: each connector provides 8 user I/Os and 3.3 V power supply connections.

The signals on IO3 and IO4 are connected via 100 Ω series resistors to the module connector, while the signals on IO2 are connected via 100 Ω series resistors to the module connector and in parallel to the FTDI (UART_RX/TX_LS) and to user LED0 and LED1. For details, refer to the Mercury+ ST1 Base Board User Schematics [4].

The I/O connector IO2 is Digilent Pmod™ compatible when VCC_IO_B and VCC_IO_A are 3.3 V.

The I/O connectors IO3 and IO4 are Digilent Pmod™ compatible when VCC_IO_A is 3.3 V.

Warning!

The I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ ST1 base board.

Warning!

Do not insert a PMOD module to these connectors if the corresponding VCC_IO_[x] supply is not 3.3 V, as this may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ ST1 base board.

4.19 Battery Holder (J1600)

A 3 V lithium battery (CR1220) can be installed for buffering the real-time clock on the connected Mercury FPGA/SoC module. The battery is not included.

Type	Manufacturer
FBA75002-S02B2101L	TXGA

Table 16: J1600 - Battery Holder Type

Warning!

There is a danger of explosion if the battery is replaced incorrectly - only replace the battery with the same or equivalent type recommended by Enclustra.

Used batteries should be disposed of according to the manufacturer's instructions.

4.20 FPGA JTAG Connector (J1502)

The FPGA JTAG connector allows accessing the JTAG port of the mounted Mercury FPGA/SoC module. The signals on this connector are protected against ESD. Series termination resistors are equipped between the module signals and the JTAG header.

Pin Number	Connection	Series Resistor
1	JTAG_TCK	22 Ω
2	JTAG_PRSNT#	-
3	JTAG_TDO	100 Ω
4	VCC_IO_A	-
5	JTAG_TMS	100 Ω
6	SRST#_RDY	100 Ω
7, 8	Not connected	-
9	JTAG_TDI	100 Ω
10	GND	-

Table 17: J1502 - FPGA JTAG Connector

JTAG_PRSNT# is used to determine if an external JTAG adapter is connected; the external adapter should tie this signal to GND when the cable is plugged in.

Warning!

The JTAG pins are connected to the FPGA/SoC device via small-value series resistors. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device. Any other voltages may damage the equipped FPGA/SoC device as well as other devices on the module or Mercury+ ST1 base board.

The JTAG connector available on the Mercury+ ST1 base board can be used in combination with Xilinx Platform Cable USB or Intel USB-Blaster download cable. For Xilinx JTAG connection, the flying wire adapter must be used.

For Intel JTAG connection, the pinout matches the Intel USB-Blaster pinout. The download cable can be connected directly to the on-board JTAG connector if the JTAG adapter is not a right-angle style (due to mechanical limitations), otherwise a flying-wire adapter is required in this case.

5 Power

5.1 Power Input

The Mercury+ ST1 base board can be powered using one of the power input sources listed below:

- External power connection through J1701 barrel jack connector
- Internal power connection through J1700 connector

5.2 Power Generation Overview

Table 18 describes the power supplies available on the base board.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Origin	Enable Signal	Power Good Signal
VCC_5V	5.0 V	2 A	Base board (VCC_MAIN)	VCC_MAIN	N/A
VCC_1V2	1.2 V	0.8 A	Module (VCC_3V3_MOD)	PWR_GOOD	POR#_LOAD#
VCC_3V3_FTDI	3.3 V	0.15 A	VCC_USBUB (primary voltage source) or VCC_3V3_MOD (secondary source)	VCC_USBUB / VCC_3V3_MOD	N/A

Table 18: Generated Power Supplies

The 3.3 V voltage coming from the Mercury module (VCC_3V3_MOD) is sequenced on the base board (VCC_3V3) using a load switch with PWR_GOOD as enable signal.

VCC_OUT_A, VCC_OUT_B and VCC_FMC_VIOB are voltage inputs to the Mercury+ ST1 base board coming from the Mercury module, respectively from the FMC card.

VCC_OUT_C voltage, generated on the Mercury module, is accessible on test point TP301. This voltage source is not used on the base board.

Warning!

The maximum available output current for each voltage supply depends on your design. Make sure that the Mercury module I/O banks and the FMC cards do not draw more current than available on the output of the DC/DC converter.

5.3 Maximum Power Budget

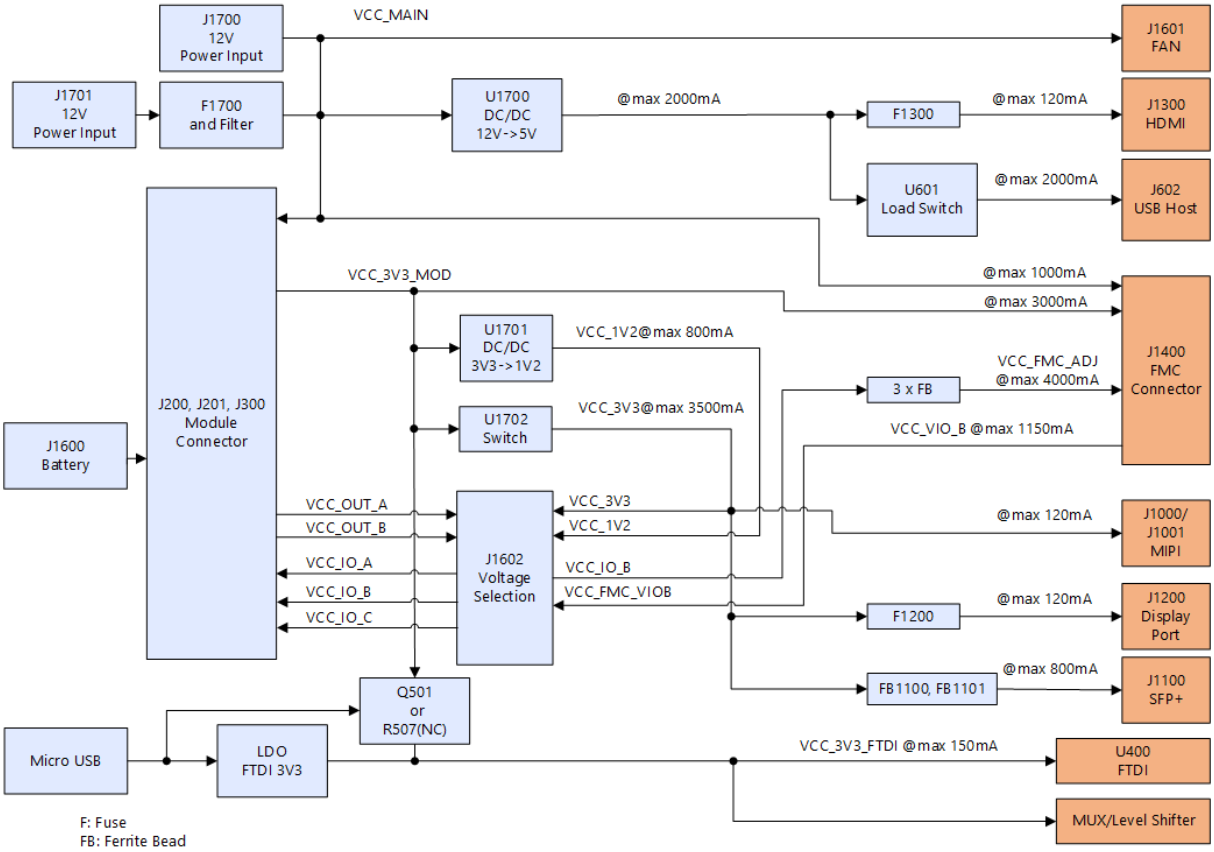


Figure 8: Maximum Power Budget Estimation

5.4 Power Sequencing

The Mercury+ ST1 base board will only power up when a Mercury module is properly connected to its socket.

As soon as the main voltage (VCC_MAIN) is applied, VCC_5V will start up and the mated Mercury module will drive up a 3.3 V supply (VCC_3V3_MOD). When this voltage becomes available on the base board, the PWR_EN signal is set to high (after a delay of 7 ms), enabling the I/O supplies on the module.

When these I/O voltages are stable, the PWR_GOOD signal goes high and the sequenced on-board 3.3 V (VCC_3V3) and 1.2 V (VCC_1V2) power domains are switched on.

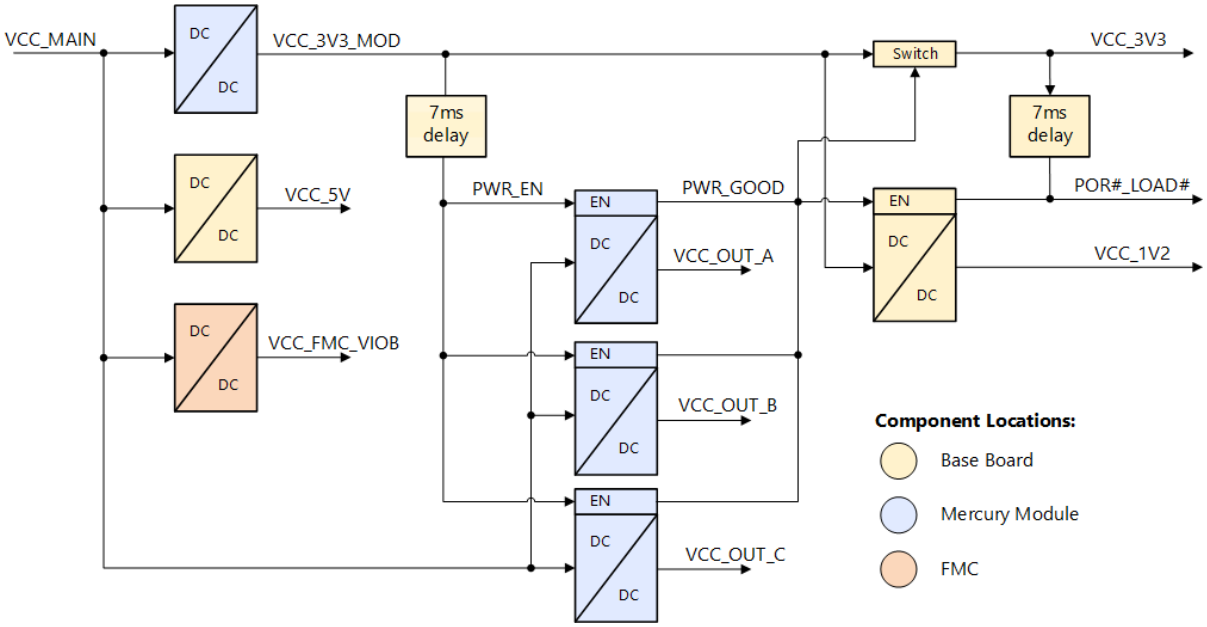


Figure 9: Power Sequence Overview

Please note that depending on the individual Mercury module, the voltage source for the DC/DC converters for the voltage outputs (VCC_OUT_*) may be different than VCC_MAIN. Refer to the module's user manual for further information on power generation on the module.

5.5 Power Enable/Power Good

The power enable signal, PWR_EN, may be used to shut down the DC/DC converters on the Mercury module - please refer to the module's user manual for details on power generation.

On the Mercury+ ST1 base board the VCC_5V supply is always active and cannot be turned-off, except for when removing the 12 V power input on the board.

The PWR_EN signal is released and no longer driven low if VCC_3V3_MOD signal is stable for 7 ms.

The PWR_GOOD signal is used for sequencing the 3.3 V voltage coming from the module - refer to Figures 8 and 9 for details.

5.6 I/O Voltage Selection

The I/O voltage selection jumpers are used to configure VCC_IO_A, VCC_IO_B and VCC_IO_C voltages that power the I/O banks of the SoC/FPGA device on the Mercury module as well as the I/O voltage VCC_FMC_ADJ for the FMC card.

The VCC_IO voltages are configurable by applying the required voltage from VCC_OUT_A, VCC_OUT_B, VCC_FMC_VIOB, VCC_1V2 or VCC_3V3 pins. This can be done by setting the I/O selection jumpers accordingly.

Tables 19, 20 and 21 describe the usage of jumpers. Please note the following:

- VCC_OUT is a supply output from the Mercury module. The value of the voltage depends on the mounted Mercury module (Refer to the "Voltage Supply Outputs" Section in the Mercury module user manual).

- VCC_FMC_VIOB is a supply output from the FMC card.
- Only one source for each I/O voltage VCC_IO_A, VCC_IO_B or VCC_IO_C is allowed.
- The factory default jumper settings are 1-2, 7-8, 11-13. As a consequence of these settings, no voltage is applied to the Mercury module connector, therefore it prevents the module from booting. PWGD LED will not be lit.

Make sure that the jumper configuration chosen does not short power nets together. The colored pins in Figure 10 represent power pins. The grey IO_ voltage pins must have a single power source.

To provide power to the VCC_IO_A, B and C pins, tree jumpers are included in the product deliverables. Please note that not all combinations can be realized with jumpers; wire jumpers can be used instead when required.

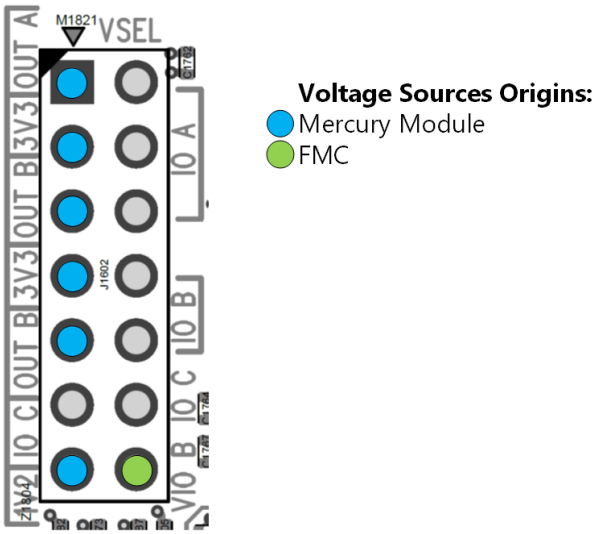


Figure 10: VCC_IO Source Pins Positions - Power Pins

Warning!

Do not merge power pins. Merging power pins can damage the Mercury module or FMC card.

Jumper Position	Source	Description
1-2	VCC_OUT_A	VCC_OUT_A is suppling VCC_IO_A
3-4	VCC_3V3	VCC_3V3 is suppling VCC_IO_A
5-6	VCC_OUT_B	VCC_OUT_B is suppling VCC_IO_A
6-8, 10-12, 11-13	VCC_1V2	VCC_1V2 is suppling VCC_IO_A & B & C

Table 19: Jumper Settings VCC_IO_A

Jumper Position	Source	Description
1-2 , 6-8	VCC_OUT_A	VCC_OUT_A is suppling VCC_IO_A & B
7-8	VCC_3V3	VCC_3V3 is suppling VCC_IO_B
9-10	VCC_OUT_B	VCC_OUT_B is suppling VCC_IO_B
9-11, 10-12	VCC_OUT_B	VCC_OUT_B is suppling VCC_IO_B & C
11-13, 10-12	VCC_1V2	VCC_1V2 is suppling VCC_IO_B & C

Table 20: Jumper Settings VCC_IO_B

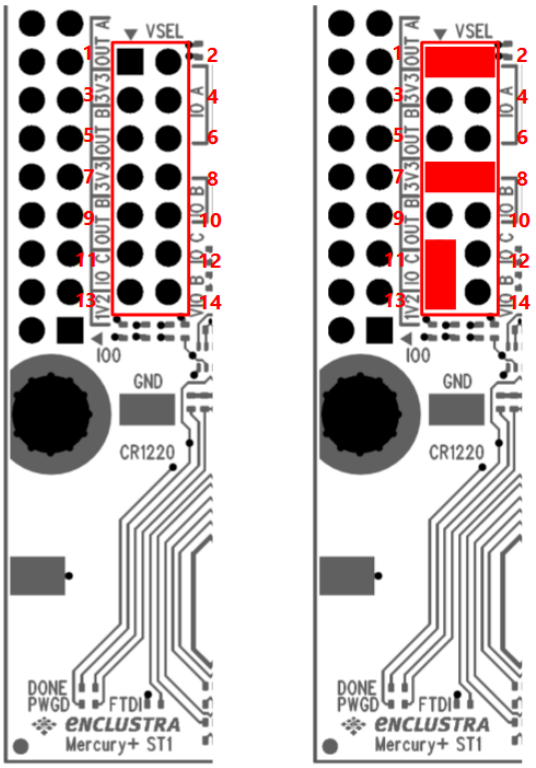
Jumper Position	Source	Description
1-2 , 6-8, 10-12	VCC_OUT_A	VCC_OUT_A is suppling VCC_IO_A, B & C
11-13	VCC_1V2	VCC_1V2 is suppling VCC_IO_C
9-11	VCC_OUT_B	VCC_OUT_B is suppling VCC_IO_C
12-14	VCC_FMC_VIOB	VCC_FMC_VIOB is suppling to VCC_IO_C

Table 21: Jumper Settings VCC_IO_C

Warning!

Use only VCC_IO_A, B and C voltages compliant with the equipped Mercury module; any other voltages may damage the equipped Mercury module, as well as other devices connected to Mercury+ ST1 base board.

Figure 11 shows the pin numbering for connector J1602 and provides one configuration example.



Example:
VCC_IO_A = VCC_OUT_A
VCC_IO_B = VCC_3V3
VCC_IO_C = VCC_1V2

Figure 11: VCC_IO Jumper Positions - Pin Numbering and Configuration Example

6 Board Function

6.1 LEDs

LED Name	LED	Signal Name	Controlled by	Description
PWGD	D1602	PWR_GOOD	Power circuits	Indicates that PWR_GOOD is active and VCC_IO_A, B, and C are available
DONE	D1601	FPGA_DONE	Mercury module	FPGA configuration is done
FTDI	D401	FTDI_LED	FTDI	Function controlled by the FTDI device
LED0	D1604	GPIO0_LED0#	Mercury module	User LED, shared with IO connector 2 (pin 2)
LED1	D1605	GPIO1_LED1#	Mercury module	User LED, shared with IO connector 2 (pin 4)
LED2	D1606	LED2	Mercury module	User LED
LED3	D1607	LED3	Mercury module	User LED

Table 22: Board LEDs

For details on the LED connections, refer to the Mercury+ ST1 Base Board User Schematics [4].

6.2 Buttons

All buttons are active-low; their function is described in Table 23.

The user buttons can be configured by the user to have various functions. For details, refer to the Mercury+ ST1 Base Board User Schematics [4].

Button Name	Button	Signal Name	Function	Comments
POR	S1600	POR#_LOAD#	Power-on reset/ Configuration-clear	Refer to the Enclustra Module Pin Connection Guidelines [8]
BTN0	S1602	BTN0#	User function	
BTN1	S1603	BTN1#	User function	Optional: shared with VCXO control voltage filter

Table 23: Board Buttons

6.3 DIP Switches

There is a 4-bit configuration switch on the Mercury+ ST1 base board. Table 24 describe its function; the factory default is marked in bold.

Warning!

Please note that the DIP switches must be configured according to the connectivity requirements. The factory default configuration does not implicitly indicate a valid configuration. The DIP switches may require different settings depending on the equipped module.

For details on the board configuration, refer to the Mercury+ ST1 Base Board User Schematics [4].

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG 1	BOOT_MODE0	**OFF**	**BOOT_MODE0 is set to 1**	Refer to the Mercury module user manual
		ON	BOOT_MODE0 is set to 0	
CFG 2	BOOT_MODE1	**OFF**	**BOOT_MODE1 is set to 1**	Refer to the Mercury module user manual
		ON	BOOT_MODE1 is set to 0	
CFG 3	USB_MODE0	OFF	USB_MODE0 is set to 1	Refer to Figure 12
		ON	**USB_MODE0 is set to 0**	
CFG 4	USB_MODE1	OFF	USB_MODE1 is set to 1	Refer to Figure 12
		ON	**USB_MODE1 is set to 0**	

Table 24: Configuration Switch

6.4 Ethernet

The Mercury+ ST1 base board is equipped with two Gigabit Ethernet ports, configured according to the capabilities of the mounted module.

The RJ45 connector with integrated magnetics is equipped on the base board, while the Ethernet PHY is equipped on the Mercury module.

6.5 USB

6.5.1 USB Overview

Figure 12 presents an overview of the USB connections on the Mercury+ ST1 base board.

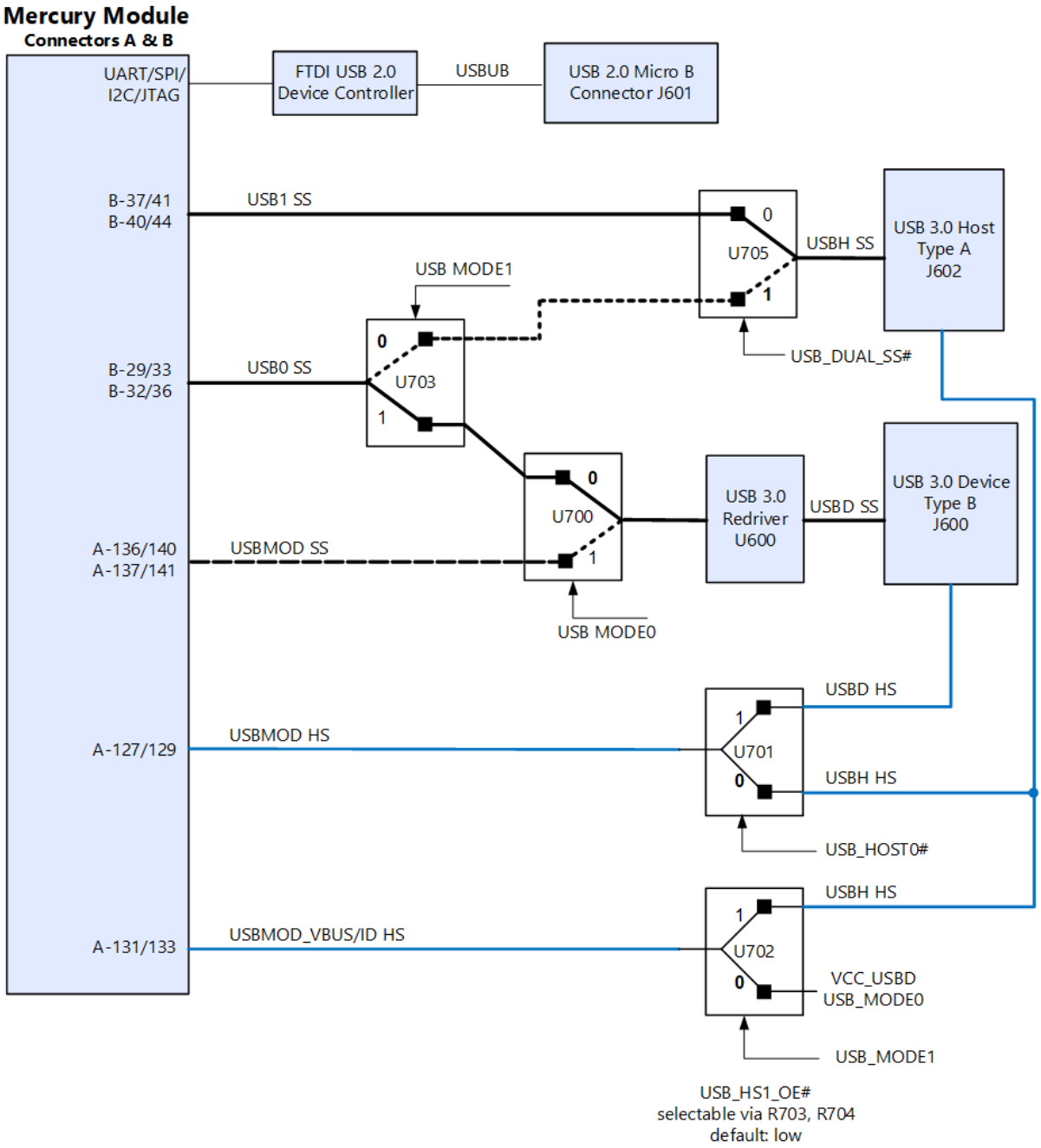


Figure 12: USB Connections Overview

Table 25 describes the connectivity options for USB on the Mercury+ ST1 base board. The default configuration is marked in bold.

USB 3.0 support is possible when the Mercury module is equipped with a Cypress FX3 USB 3.0 device controller or when the module is equipped with a Zynq Ultrascale+ device with USB 3.0 support on the PS GTR

transceivers.

The USB 2.0 connectivity options offer compatibility with both modules having a single USB interface (USB controller or USB OTG support) or modules having two USB interfaces.

Appendix A describes the supported use cases and configuration examples for the available Mercury modules.

USB_MODE1 CFG DIP 4	USB_MODE0 CFG DIP 3	HS0 A-127/129	HS1/VBUS A-131/133	FX3 SSRX/TX A-136/140 A-137/141	MGT2/SS B-29/33 B-32/36	MGT3/SS B-37/41 B-40/44
On	**On**	USB-A	VBUS/ID	-	USB-A	-
On	Off	USB-B	VBUS/ID	USB-B	USB-A	-
Off	On	USB-B	USB-A	-	USB-B	USB-A
Off	Off	USB-B	USB-A	USB-B	-	-

Table 25: USB Connection Table

The USB 2.0 micro B connector on the front panel is connected solely to the FTDI device. This connection can be used for configuration or test purposes.

6.5.2 USB 2.0 Device Controller (FTDI)

The Mercury module FPGA configuration interface and QSPI flash signals are connected to the FTDI USB 2.0 device controller. This allows FPGA serial configuration and SPI flash programming over USB from a host computer without additional hardware.

Port A of the FTDI device is used for Xilinx JTAG implementation.

Port B of the FTDI is used to access the I2C bus and the UART pins of the Mercury module, to program the SPI Flash or to configure the FPGA in slave serial mode. General purpose I/O pins of port B (FTDI_MODE0/1) are used to control the configuration multiplexers; refer to Table 26 for details.

By default, the UART communication between the FTDI device and FPGA is active. The Xilinx JTAG mode can be activated using the Enclustra MCT [10] and is independent of the UART connection.

The library used by the MCT is available free of charge; it allows users to integrate module enumeration, FPGA and SPI flash configuration, and I2C communication functionality in their own application. The library consists of a Windows DLL with a C-style interface, allowing use of the library from almost any programming language; for C++ applications, a C++ wrapper is also provided. Please contact Enclustra for details.

FTDI_MODE1 (BCBUS6)	FTDI_MODE0 (BCBUS5)	BOOT_MODE0 (BCBUS4)	Configuration
0	0	1	Slave serial configuration via FTDI
0	1	X	FTDI device pins connected to module I2C bus
1	0	0	SPI flash programming via FTDI
X	1	0	Master serial configuration (Mercury module is configured from SPI flash)
1	1	X	FTDI device pins connected to Mercury module UART pins

Table 26: FTDI Configuration Settings - Port B

The control signals FTDI_MODE0 and FTDI_MODE1 are used to configure the way BDBUS0-3 pins are routed on the module: to UART, I2C, SPI flash or Mercury module SPI configuration port.

Please note that for the SPI flash programming SRST#_RDY# (BCBUS2) must be pulled low. For the slave/-passive serial configuration BOOT_MODE0 must be pulled high or left open, while for master/active serial configuration BOOT_MODE0 must be pulled low.

Warning!

After Mercury module slave/passive serial configuration or SPI flash programming operations, the FTDI_MODE0 signal must be pulled high, to avoid damaging the equipped Mercury module device.

6.6 I2C Communication

There are several I2C devices on the Mercury+ ST1 base board connected to two separate I2C buses. The Mercury module and the FTDI device can be I2C masters on the main I2C bus. An overview of the I2C structure is given in Table 27 and Figure 13. The I2C devices located on the Mercury module are shown in a dashed box in Figure 13.

Please note that all I2C addresses are written in a 7-bit hexadecimal format.

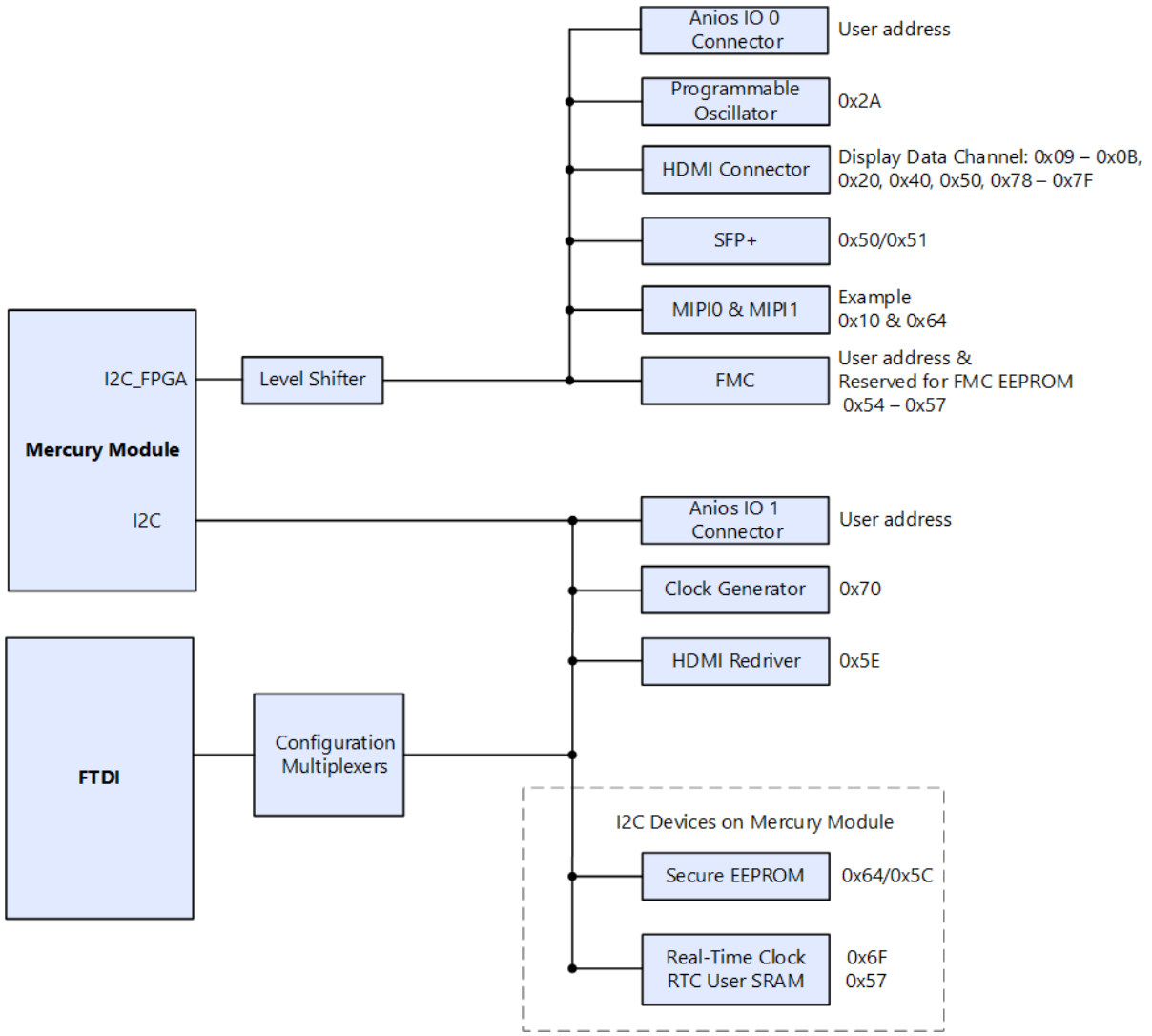


Figure 13: I2C Devices

The I2C_SCL_FPGA and I2C_SDA_FPGA signals are connected with 0 Ω resistor jumpers to HDMI and FMC connectors.

The programmable oscillator Si570 is not equipped on the Mercury+ ST1 base board by default, therefore the address space 0x2A is not automatically occupied.

Board Reference / Pin	I2C Net Name	Comments
J200 / A-55	I2C_SCL_FPGA	Signal is level shifted to 3.3 V
J200 / A-57	I2C_SDA_FPGA	Signal is level shifted to 3.3 V
J200 / A-111	I2C_SCL	
J200 / A-113	I2C_SDA	
J200 / A-115	I2C_INT#	Connected to Anios connectors and clock generator on the base board
U505 / 2	I2C_SCL	Connected to FTDI device when the FTDI mode setting is [0,1]
U505 / 5, 11	I2C_SDA	Connected to FTDI device when the FTDI mode setting is [0,1]

Table 27: I2C Structure

6.7 HDMI

The Mercury+ ST1 base board supports HDMI 1.4b and 2.0b output signals. The display data channel (DDC) for audio and video format recognition is wired to the I2C FPGA bus (pins A-55/57). The standard I2C bus (A-111/113) is used for the redriver configuration.

The three HDMI data lanes are routed to the Mercury module connector C (C-45/47, C-51/53, C-57/59) to be connected to transceivers for modules having MGTs on these pins. By default the clock connection is made to pins C-139/141. If the application requires having the clock mapped to the 4th MGT channel of the same quad as the data lanes (pins C-63/65), it is possible to realize this connection by removing resistors R310 - R313 and by populating R308 - R309. In this case, the SFP+ port is not available any longer.

The HDMI redriver equipped on the board performs pair deskew, therefore the configuration of three MGT lanes and a TMDS clock (allowing for the additional SFP+ port) is supported.

This interface is protected against electrostatic discharge by using TVS diodes.

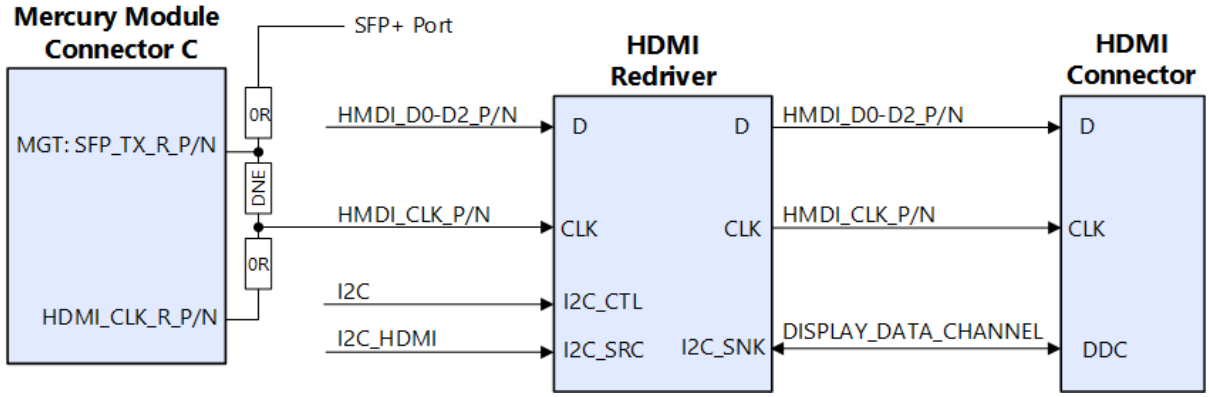


Figure 14: HDMI Connector with Redriver

6.8 DisplayPort

The main link of the DisplayPort interface consists of two lanes, driven directly by the MGT signals on connector B (pins B-13/17, B-21/25).

Lanes 0 and 1 are mapped directly to the transmitter side of the MGTs, while lane 2 and 3 are mapped to MGT receivers. This allows a full duplex link between two individual Mercury+ ST1 base boards by connecting a mini DisplayPort cable, for example for debugging or performance evaluation purposes.

For the traditional DisplayPort applications the following connections are used: MGT transmitter lanes 0 and 1, along with an auxiliary channel (pins A-88/90/92) and a hot plug detect signal (pin A-94). The translation between LVTTL and LVDS is done with a dedicated transceiver.

The supported DisplayPort standard is dependent on the connected Mercury module.

This interface is protected against electrostatic discharge by using TVS diodes.

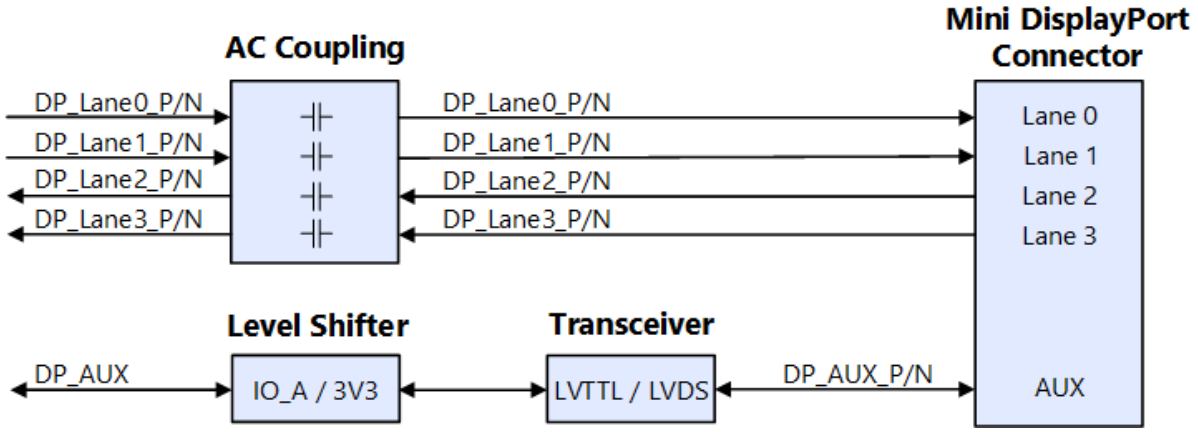


Figure 15: Mini DisplayPort Connector with LVDS Transceiver

6.9 MIPI

Two MIPI (Mobile Industry Processor Interface) standard interfaces are available to the user. Default application supports two CSI (Camera Serial Interface), MIPI0 and MIPI1, with two data lanes each. The form factor allows to connect two low-cost Raspberry Pi cameras.

The MIPI pinout for both CSI interfaces has been checked to work optimally with the Mercury+ XU7, XU8 and XU9 SoC modules. The pinout respects the RX rules indicated by the MIPI D-PHY IP core documentation [11].

The connector used for MIPI1 may optionally be connected to a two-lane capable display. To attach a Raspberry Pi display, the lanes should be mapped according Table 28, column DSI mapping. Please note that depending on the attached display the signal mapping may differ from the proposed permutations.

Board Reference / Pins	CSI mapping	DSI mapping
J1001 / 7,8	Clock	Data Lane 0
J1001 / 10,11	Data Lane 1	Clock
J1001 / 13,14	Data Lane 0	Data Lane 1

Table 28: MIPI Connector 1 CSI / DSI Signal Mapping - Rasperry Pi Display Lane Mapping

Figure 17 shows the connections for the CSI and DSI use cases. When the MIPI interface is used as CSI, the FPGA I2C bus is used as camera control interface (CCI).

In case of a DSI interface, the pins corresponding to I2C may be used for power - please read carefully the datasheet of the connected MIPI device to check the connectivity requirements.

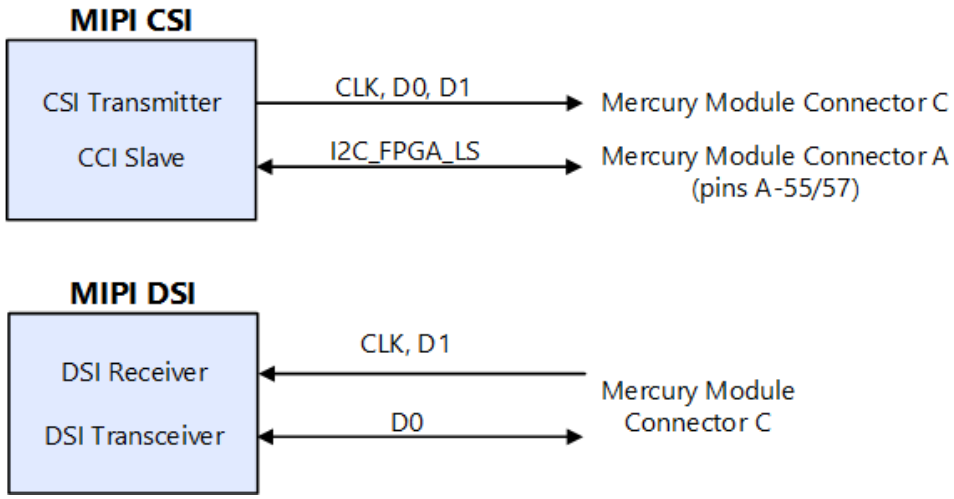


Figure 16: MIPI CSI/DSI Interface with Zynq UltraScale+ Modules

When a display is used for MIPI1 interface, the FPGA I2C must be connected to MIPI0 interface (for the CCI function) leaving the I2C MIPI1 pins available for the power connections - refer to Table 29.

The I2C for the camera interfaces may be selected via I2C_MIPI_SEL signal.

I2C_MIPI_SEL Value	MIPI I2C Active	I2C_SDA_MIPI1 State
0	MIPI0	VCC_3V3
1	MIPI1	I2C_SDA_FPGA_LS

Table 29: MIPI I2C Bus Selection and Connectivity Options

For use with older FPGA families that do not natively support SLVS IO standard (Zynq-7000, 7-series, Cyclone V) hardware changes are required in order to provide proper signal termination and tap the high-speed signals to dedicated FPGA inputs. Low-power signaling is supported only for lane 0 (D0). Clock and data 1 support only the high-speed mode.

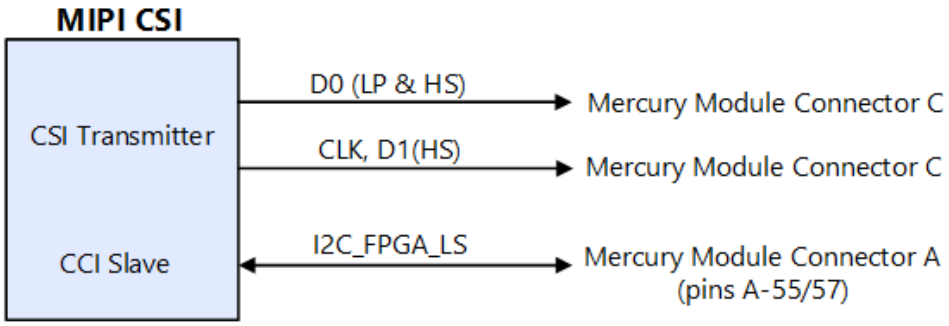


Figure 17: MIPI CSI Interface with Zynq-7000/7-Series Modules

Tables 30 and 31 describe the hardware changes required to operate the MIPI CSI interfaces in combination with older FPGA families. By default module connector pins: C-160/162, C-145/147 and C-154/156 are used for MIPI 0, while pins C-161/163, C-164/166 and C-157/159 are used for MIPI 1.

The clock pairs on module connector pins C-151/153 and C-148/150 respectively are only used for older FPGA families, such as Zynq-7000 series.

FPGA Family	Remove	Equip
Zynq Ultrascale+	-	-
Zynq-7000 (and similar Intel FPGA families)	R1005 - R1006	R1007 - R1013

Table 30: MIPI Connector 0 CSI - Hardware Changes for older FPGA Families

FPGA Family	Remove	Equip
Zynq Ultrascale+	-	-
Zynq-7000 (and similar Intel FPGA families)	R1019 - R1020	R1021 - R1027

Table 31: MIPI Connector 1 CSI - Hardware Changes for older FPGA Families

6.10 Clock Architecture

The Mercury+ ST1 base board provides the user with a diversity of clock configuration options. The board is equipped with a clock generator programmable via I2C having as reference a 100 MHz clock from an oscillator (Y801). Alternatively, a user oscillator (Y800) with another frequency can be used as reference - this part is not equipped by default on the board.

The Mercury+ ST1 base board may be optionally equipped with a voltage-controlled oscillator (Y802) - this part is not equipped by default.

Figure 18 describes the clocking architecture available on the board. For further information please refer to the Mercury+ ST1 Base Board User Schematics [4].

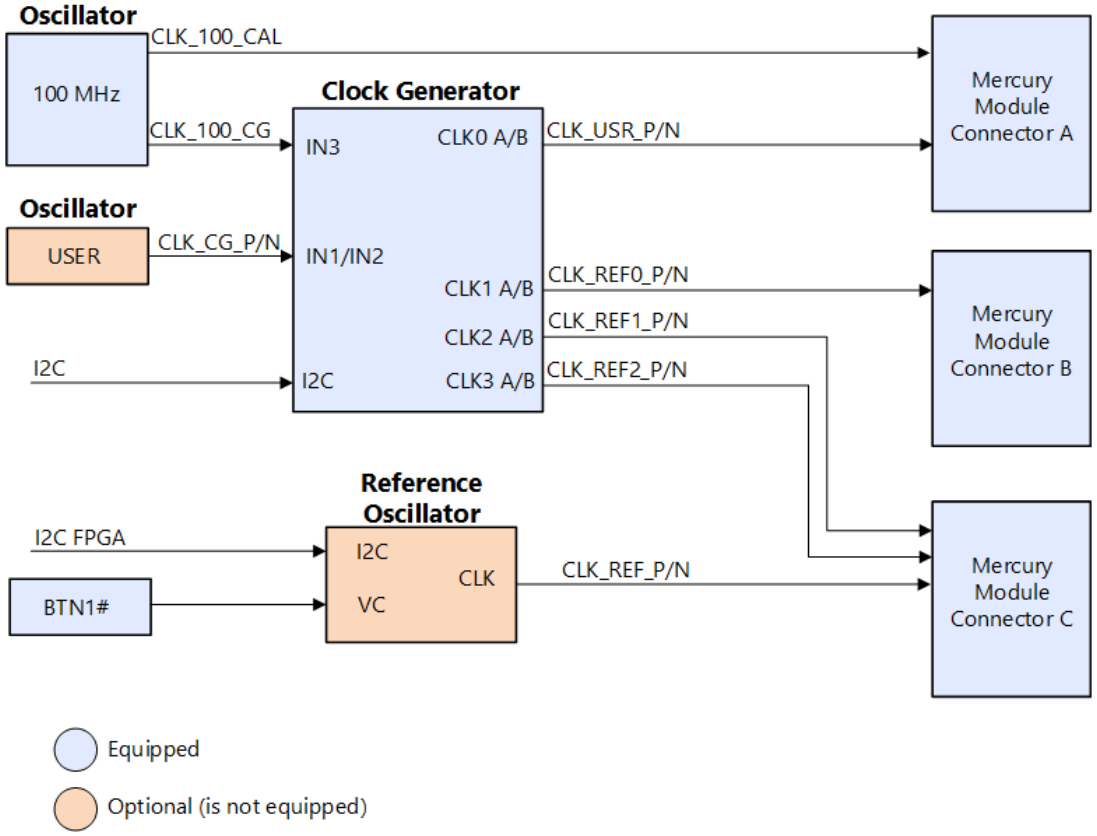


Figure 18: Clock Architecture Overview

6.10.1 Clock Generator

The Mercury+ ST1 base board features a clock generator circuit addressable and configurable via I2C.

Type	Manufacturer
Si5338B-B-GMR	Silicon Labs

Table 32: Clock Generator Type

The clock generator has to be configured at power-up via I2C by the Mercury module or by another I2C master. The device also provides the option of storing a user-defined clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up. The NVM is a one-time programmable (OTP) memory.

The Si5338B device can be reconfigured to desired functionality via the I2C interface. ClockBuilder ™ Desktop Software is a tool provided by Silicon Labs, which allows the user to specify several settings, such as the input clock pins and clock frequency, the output clock frequencies and phase shifts. These settings can be exported and used in the software code to configure the clock generator.

For details on features and configuration, refer to the Si5338B datasheet.

Warning!
Writing the contents of the NVM OTP configuration memory voids the board warranty.

7 Operating Conditions

7.1 Absolute Maximum Ratings

Table 33 indicates the absolute maximum ratings for Mercury+ ST1 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	-0.3 to 16	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mercury module user manual	
$T_{ambient}$	Ambient temperature range for wide range boards (W) *	-20 to +75	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 33: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Table 34 indicates the recommended operating conditions for Mercury+ ST1 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	12	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mercury module user manual	
$T_{ambient}$	Ambient temperature range for wide range boards (W) *	-20 to +75	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 34: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

8 Ordering and Support

8.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

8.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

References

[1] Enclustra General Business Conditions
http://www.enclustra.com/en/products/gbc/
[2] Enclustra FPGA Manager IP Solution
http://www.enclustra.com/en/products/fpga-manager/
[3] Mercury+ ST1 Base Board IO Net Length Excel Sheet
→ Ask Enclustra for details
[4] Mercury+ ST1 Base Board User Schematics
→ Ask Enclustra for details
[5] Mercury+ ST1 Base Board Known Issues and Changes
→ Ask Enclustra for details
[6] Mercury+ ST1 Base Board 3D Model (PDF)
→ Ask Enclustra for details
[7] Mercury+ ST1 Base Board STEP 3D Model
→ Ask Enclustra for details
[8] Mercury Mars Module Pin Connection Guidelines
→ Ask Enclustra for details
[9] Enclustra Mercury Master Pinout
→ Ask Enclustra for details
[10] Enclustra Module Configuration Tool
http://www.enclustra.com/en/products/tools/module-configuration-tool/
[11] MIPI D-PHY v4.1, LogiCORE IP Product Guide, Vivado Design Suite, PG202, v1.4, Xilinx

A Appendix

Use Scenario	Module	USB MODE1	USB MODE0	USB HS1_OE#	USB-B	USB-A	USB HS0	USB HS1	PS MGT2 SS USB0	PS MGT3 SS USB1	FX3 SS
	e.g.	*DIP Switch*	*DIP Switch*	*Logic*	*seen from connector*	*seen from connector*	*seen from module*	*seen from module*	*seen from module*	*seen from module*	*seen from module*
1A) Single HS USB[1] **1B)** Single HS USB[2] as host	ZX1, ZX5, SA1 XU1/5/6 XU7/8/9	On	On	0[3]	-	USB-HS0	USB-A	VBUS	USB-A	-	-
2) Single HS USB Module using USB-B (option with FX3)	KX1 KX2 CA1	On	Off	0	USB-HS0	-	USB-B	VBUS	USB-A	-	USB-B
3) Dual HS USB Module (option with PS SS0 and SS1)	XU1, XU7 XU5, XU6 XU8, XU9	Off	On	0	USB-HS0	USB-HS1	USB-B	USB-A	USB-B	USB-A	-
4) Dual HS USB Module using USB-B (option with FX3)	AA1 SA2	Off	Off	0	USB-HS0	USB-HS1	USB-B	USB-A	-	-	USB-B

Table 35: USB Use Case Scenario

[1] Single HS USB Module, without SS, using USB-A
[2] XU* with HS1 not active and HS0/PS SS USB0 as host using USB-A
[3] Solder option resistors R703 (DNE), R704 default = 0 (use case 1A and 1B "out-of-specification" by connecting unused USB DP to 5V)