Mercury+ PE3 Base Board

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ PE3 base board to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ PE3 base board.

Summary

This document first gives an overview of the Mercury+ PE3 base board followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-PE3	Mercury+ PE3 Base Board

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-420-001	02	17.11.2022

Approval Information	Name	Position	Date
Written by	RLOC, MKON	Design Engineer	09.03.2022
Verified by	TVOE	Design Expert	18.03.2022
Approved by	IJOS	Manager, BU SP	17.11.2022

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Document History

Version	Date	Author	Comment
02	17.11.2022	MKON, TKAU, TVOE	Improve and add information in sections: Power, LED, I2C, Clock, USB, MGT and SC.
01	21.03.2022	RLOC, MKON	Version 01, preliminary

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1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ PE3 base board is equipped with a multitude of I/O connectors for use with Mercury family FPGA and SoC modules. The board is well-suited for rapid prototyping and for building FPGA systems, without the need for developing custom hardware.

The board can also be used for production flash programming on Mercury modules, or for educational purposes.

The main features of the Mercury+ PE3 base board are:

- PCIe Gen3 ×8 interface
- Support for USB 3.0 host
- USB Type-C connector with support for DisplayPort, USB 3.0 with DRP and DRD
- FTDI USB 2.0 High-Speed device controller
- High-speed FPGA and flash programming over USB
- FMC HPC Connector
- 2 × Ethernet RJ45 connectors
- 4 × SFP+ slots
- QSFP+ slot
- HDMI 2.0a connector
- M.2 SATA/NVMe slot
- FireFly connector
- System controller with built-in USB support for JTAG, SPI flash programming, UART and I2C
- Low-jitter clock generator
- microSD card slot
- Simple integration by using a single 12 V voltage supply (standalone configuration)
- Alternative power supply over PCIe connector (PCIe configuration)
- Alternative power supply via USB Type-C

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

1.1.3 RoHS

The Mercury+ PE3 base board is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury+ PE3 base board must be properly disposed of at the end of its life. If a battery is installed on the board, it must also be properly disposed of.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ PE3 base board.

1.1.5 Safety Recommendations and Warnings

Mercury boards are not designed to be "ready for operation" for the end-user. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing a Mercury module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the board and to the equipped module.

Warning!

It is possible to mount some Mercury modules the wrong way round on the Mercury+ PE3 base board - always check that the mounting holes on the base board are aligned with the mounting holes of the module.

Every Mercury module has a 1 mm copper square module marker, which has its counter part on the base board. If these module markers are aligned, proper orientation is granted. The copper square can be found in a corner of the module, on top as well as on the bottom side.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

Warning!

Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

Always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ PE3 base board. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ PE3 base board is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Deliverables

- Mercury+ PE3 base board
- Mercury+ PE3 base board documentation, available via download:
    - Mercury+ PE3 Base Board User Manual (this document)
    - Mercury+ PE3 Base Board IO Net Length Excel Sheet [3]
    - Mercury+ PE3 Base Board User Schematics (PDF) [4]
    - Mercury+ PE3 Base Board Known Issues and Changes [5]
    - Mercury+ PE3 Base Board 3D Model (PDF) [6]
    - Mercury+ PE3 Base Board STEP 3D Model [7]
    - Mercury Mars Module Pin Connection Guidelines [8]
    - Mercury Master Pinout [9]

1.3 Accessories

The following accessories are not included in the Mercury+ PE3 base board, but are required to use it.

- Mercury FPGA or SoC module
- 12 V DC/2.5 A power supply
- USB 2.0 A to micro-B USB cable

2 Getting Started

This section contains essential information on using the Mercury+ PE3 base board.

Electrostatic discharge (ESD) may damage the Mercury+ PE3 base board partially or completely. Please follow the relevant guidelines for ESD-safe handling when operating or assembling electronic components.

Before first use of the Mercury+ PE3 base board with a Mercury or Mercury+ module, the following steps must be followed:

- Mount the module on the module slot on the base board, with the power switched off.

Warning!

It is possible to mount some Mercury modules the wrong way round on the Mercury+ PE3 base board - always check that the mounting holes on the base board are aligned with the mounting holes of the module.

Every Mercury module has a 1 mm copper square module marker, which has its counter part on the base board. If these module markers are aligned, proper orientation is granted. The copper square can be found in a corner of the module, on top as well as on the bottom side.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

Warning!

Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

Always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ PE3 base board. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

- Set the DIP switches correctly (refer to Section 6.5).
- Set the I/O voltage selection jumpers correctly (refer to Section 5.5).
- Power up the board (refer to Section 5 for power options).

The power supply of the base board must be turned off in the following situations:

- Before changing the position of the I/O voltage selection jumpers
- Before removing the Mercury or Mercury+ module
- Before connecting or disconnecting peripherals to ANIOS and I/O connectors
- Before connecting or disconnecting FMC cards

Before connecting peripherals, make sure that the corresponding VCC_IO voltage is properly set.

The operating conditions for the Mercury+ PE3 base board and equipped module must conform to the values given in Section 7, and in the relevant section from the Mercury or Mercury+ module user manual.

Warning!

The Mercury+ PE3 base board can only be used in combination with a Mercury or Mercury+ module. Using the board without module will cause the "FAIL" LED to turn on; refer to Section 6.7 for details.

3 Board Description

3.1 Block Diagram

The Mercury+ PE3 base board is available in two different hardware configurations:

- ME-PE3-C (1 × FMC connector, 1 × QSFP+ connector)
- ME-PE3-4S-C (1 × FMC connector, 1 × QSFP+ connector, 4 ×SFP+ connectors)

The Mercury+ PE3 base board can be used in combination with any Mercury module. Depending on the equipped module some features may not be available.

The block diagram of the Mercury+ PE3 base board is shown in figure 1.

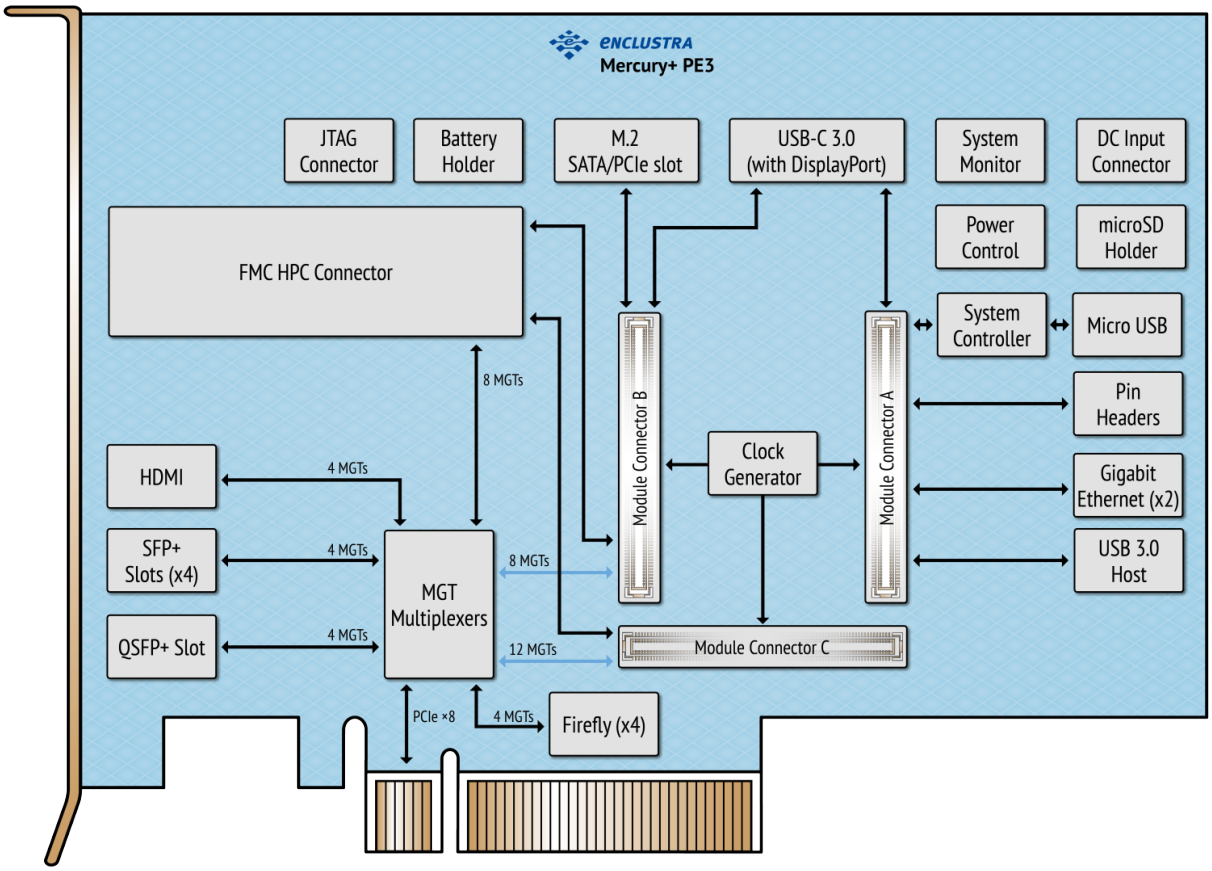


Figure 1: Hardware Block Diagram ME-PE3-4S-C

3.2 Features

Table 1 describes the features available on the Mercury+ PE3 base board.

Feature	Description
Form factor	171 × 112.4 mm
Module connector	3 × Number of 168-pin Hirose FX10 connectors
System features	System controller Built-in USB support for Xilinx JTAG, SPI flash programming and UART and IC2 System monitor Power control Current sense Flexible MGT routing between Mercury connector and MGT capable endpoints Low-jitter clock generator Programmable user oscillator (optional) 1 × Custom clock inputs (micro-coaxial connection) 7 × Status LEDs Battery holder to supply RTC on module
Memory	microSD card holder User EEPROM
Connectors	PCIe ×8 interface QSFP+ slot 4 ×SFP+ slots (only for ME-PE3-4S-C product model) HDMI 2.0a connector USB Type-C connector USB 3.0 host interface Micro USB 2.0 device (UART, SPI, I2C, JTAG) interface 2 × Ethernet RJ45 connectors M.2 SATA/NVMe slot FireFly connector FMC HPC connector JTAG connector Fan connector

Continued on next page...

Feature	Description
User I/Os	40-pin Anios pin header 2 × Digital IO connectors (micro-coaxial connection) shared with LEDs 1 × User push button 6 × User LEDs (2 shared with digital IO connectors)
Powering options	12 V barrel jack USB Type-C power PCIe connector

Table 1: Base Board Features

Warning!

Please note that the available features depend on the equipped Mercury FPGA/SoC module.

3.3 Board Configuration and Product Models

Table 2 describes the standard base board configurations. Custom configurations are available; please contact Enclustra for further information.

Product Model	4 ×SFP+ connectors	QSFP+ connectors	FMC HPC connectors	Temperature Range
ME-PE3-C	✗	✓	✓	-10 to +75° C
ME-PE3-4S-C	✓	✓	✓	-10 to +75° C

Table 2: Standard Base Board Configuration

3.4 EN-Numbers and Part Names

Every board is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 2.

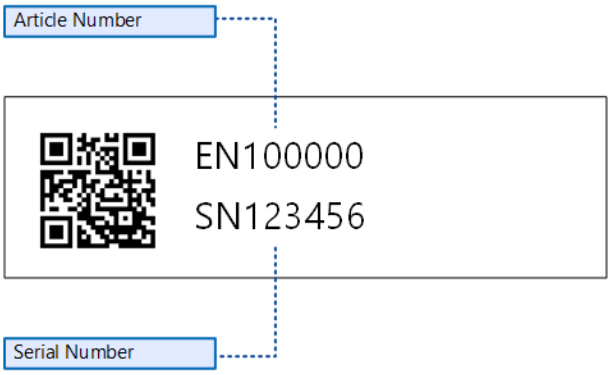


Figure 2: Product Label

The correspondence between EN-number and part name is shown in Table 3. The part name represents the product model, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury+ PE3 Base Board Known Issues and Changes document [5].

EN-Number	Part Name
EN103035	ME-PE3-C-R1.0
EN103036	ME-PE3-4S-C-R1.0

Table 3: EN-Numbers and Part Names

3.5 Top and Bottom Views

3.5.1 Top View

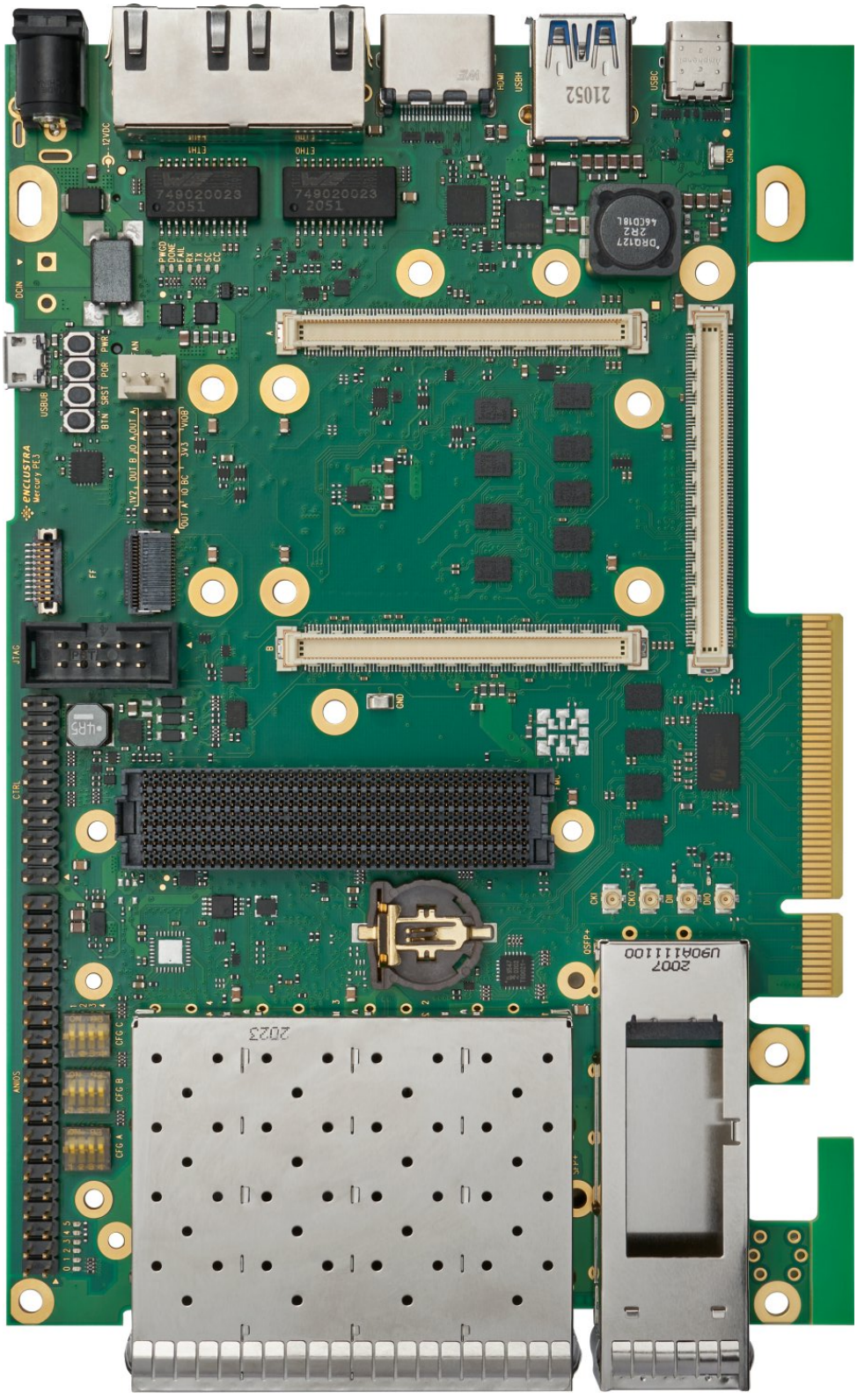


Figure 3: Board Top View ME-PE3-4S-C-R1.0 with 4 ×SFP+ Connectors

3.5.2 Bottom View

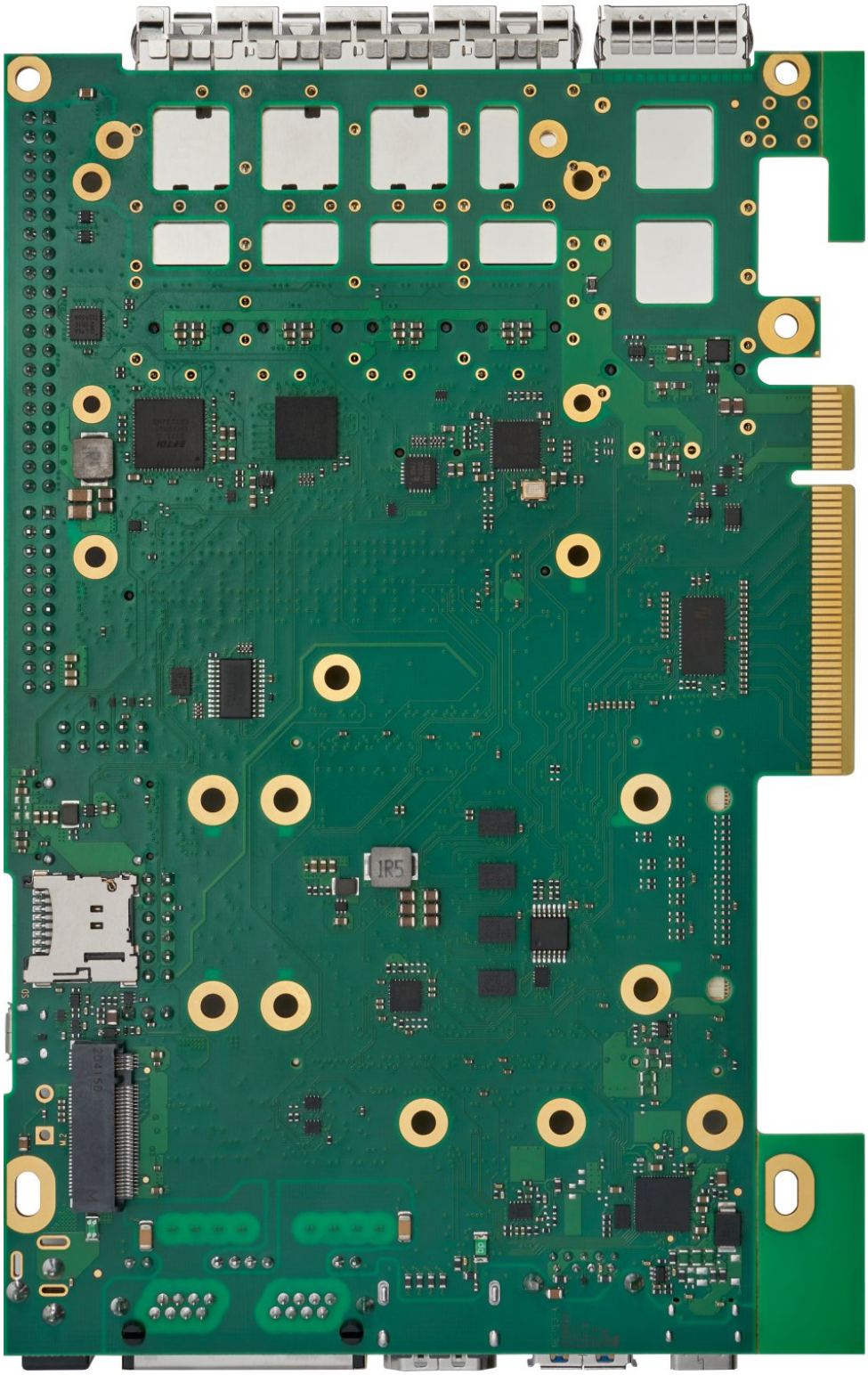


Figure 4: Board Bottom View ME-PE3-4S-C-R1.0 with 4 ×SFP+ Connectors

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.6 Top and Bottom Assembly Drawings

3.6.1 Top Assembly Drawing

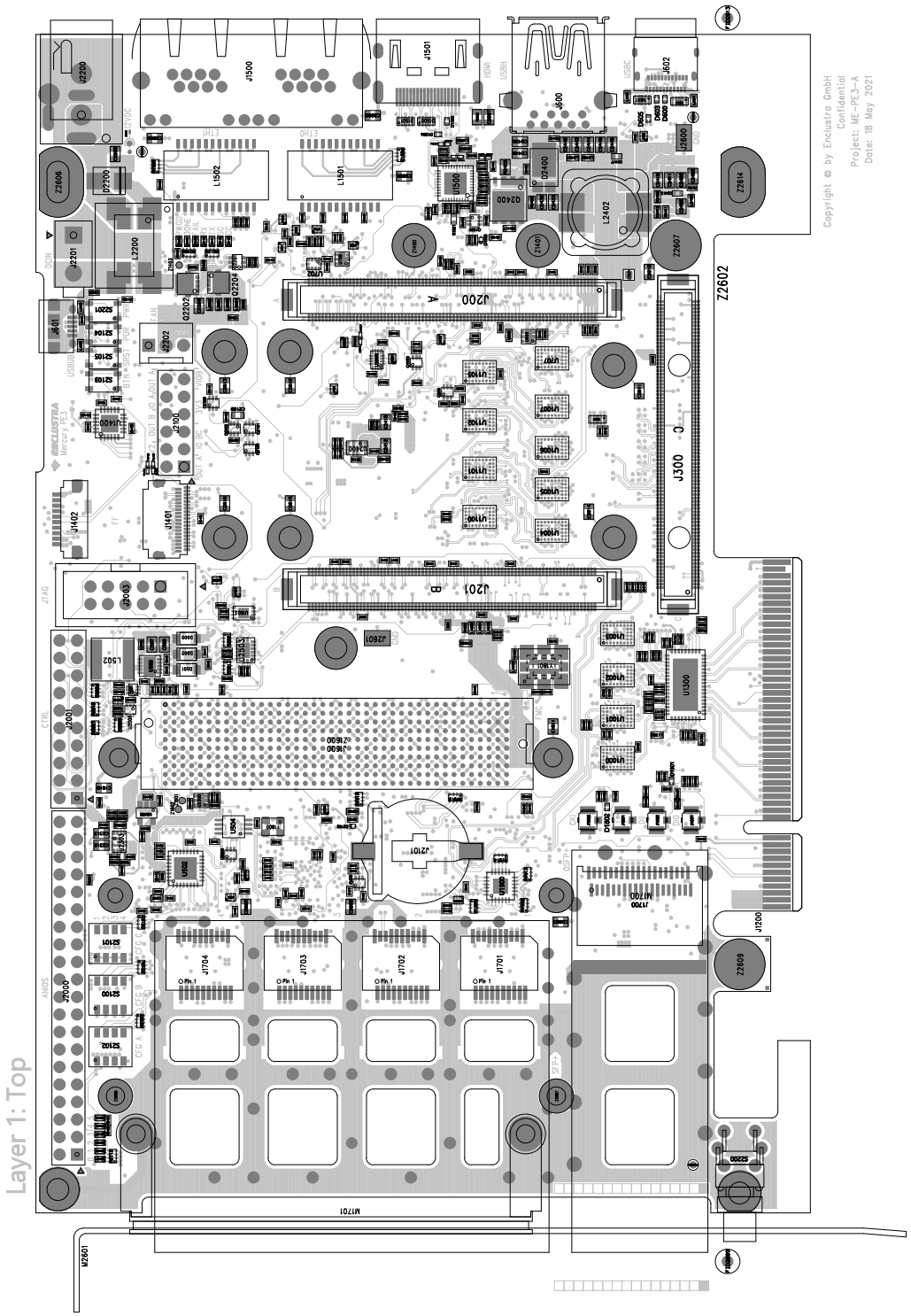


Figure 5: Board Top Assembly Drawing

3.6.2 Bottom Assembly Drawing

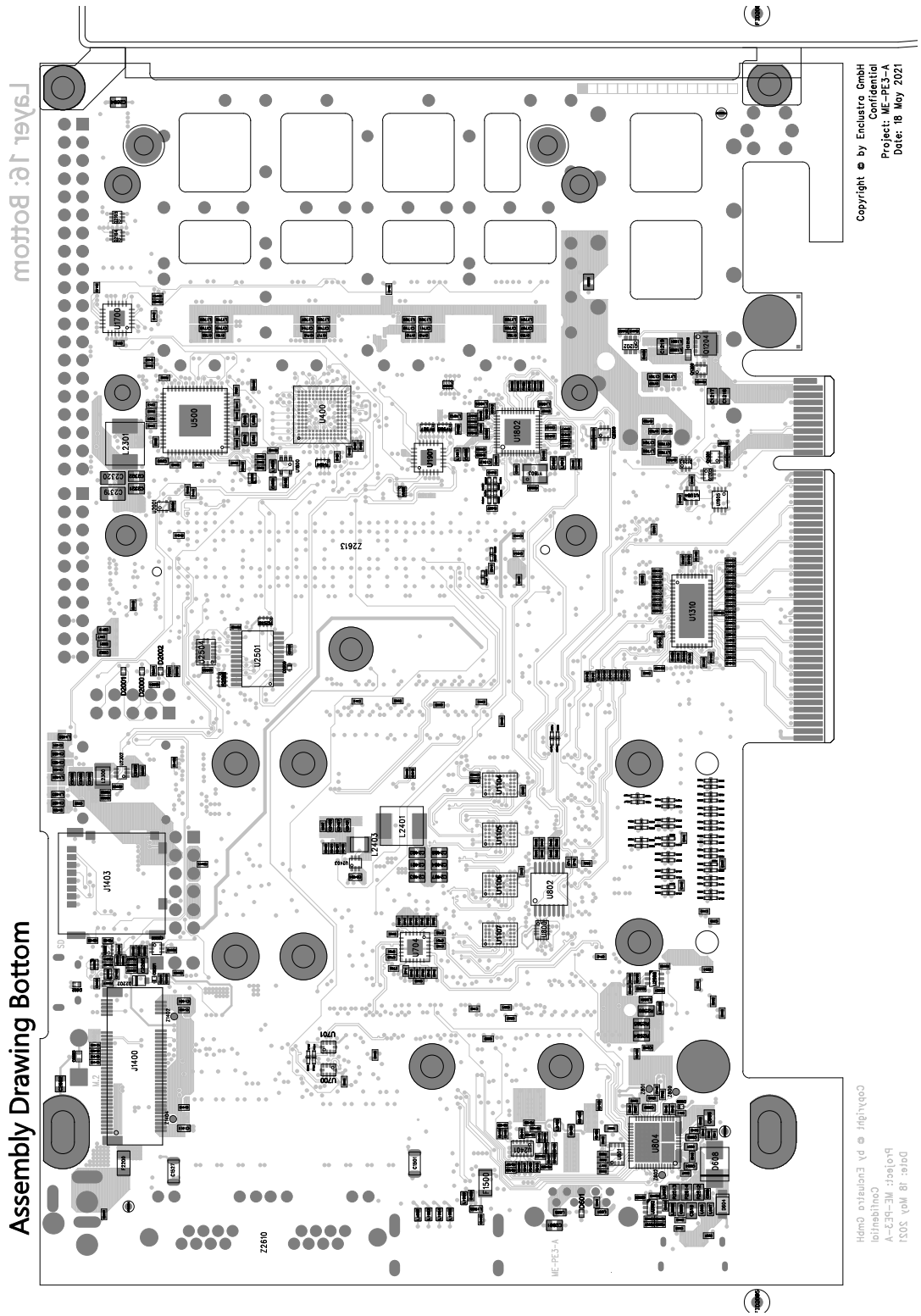


Figure 6: Board Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.7 Board Dimensions

Detailed information on board dimensions can be found in the STEP 3D model [7].

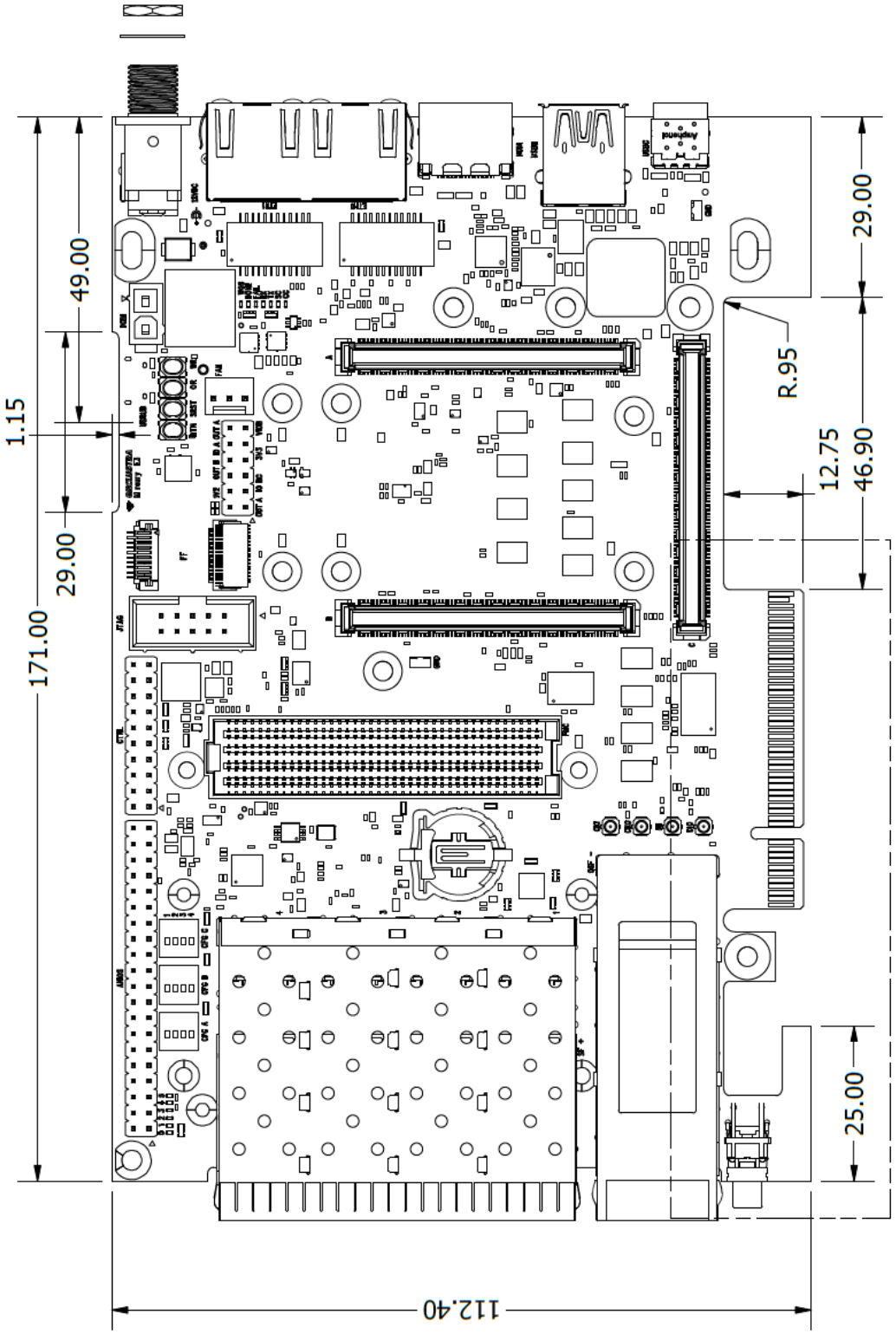


Figure 7: Board Dimensions

3.8 Mechanical Data

Table 4 describes the mechanical characteristics of the Mercury+ PE3 base board. A 3D model (PDF) and a STEP 3D model are available [6], [7].

Symbol	Value
Size	171 × 112.4 mm
Component height top	13.46 mm
Component height bottom	4.2 mm
Weight	146 g (without battery, module and bracket)

Table 4: Mechanical Data

3.9 Mechanical Components

Table 5 describes the mechanical components present on the Mercury+ PE3 base board. The listed elements are for reference only. Any other components that meet the requirements may be used.

Product Number	Manufacturer	Description
970080365	Würth Elektronik	5 × plastic spacer bolt with female/female thread M3, length 8 mm, beneath Mercury module
970070365	Würth Elektronik	2 × plastic spacer bolt with female/female thread M3, length 7 mm, beneath Mercury module
MPMS 003 0008 PH	B&F Fastener Supply	5 × Phillips pan head metric screws M3x8

Table 5: List of Mechanical Components

4 Connectors Description

The Mercury+ PE3 base board has wide variety of different connectors. The following figures show the placement of the connectors on the board. Most of the connectors are on the top of the Mercury+ PE3 base board, just the SD card and M.2 slot are on the back. The following section describes each connector and specifies its capabilities.

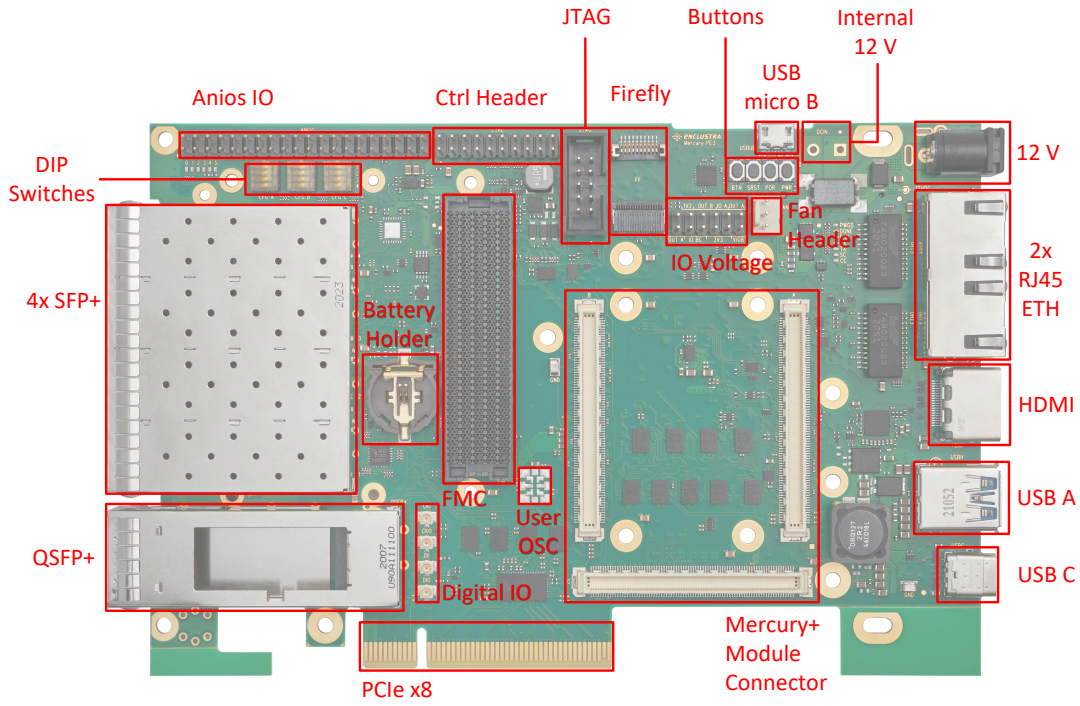


Figure 8: Connectors Top

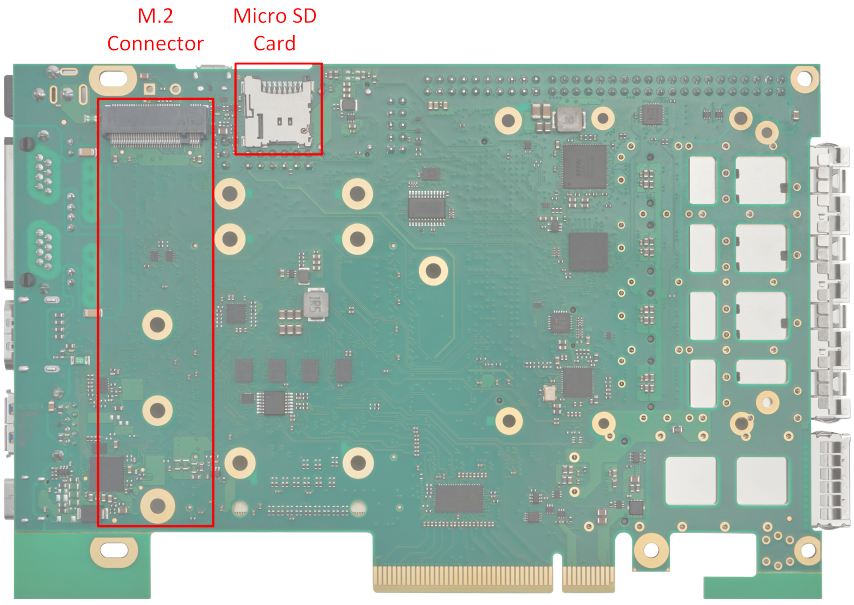


Figure 9: Connectors Bottom

4.1 12 V External Power (J2200)

This connector is used to supply the main VCC input voltage, when the Mercury+ PE3 base board is not powered via PCIe or USB Type-C.

Apply only 12 V DC to this connector. There is a 12 A Fuse F2200 in series to this connector.

Pin Number	Signal Name	Description
1 (inner)	VCC_MAIN_IN	12 V DC (nominal) input voltage
2 (outer)	GND	Ground

Table 6: J2200 - External Power Connector

Table 7 lists the power connector types used on the Mercury+ PE3 base board.

Type	Manufacturer	Description	Assembly
PJ-102AH	CUI	Power Jack 5 A	Default
RASPC10P	Switchcraft	Power Jack 11 A	Option

Table 7: J2200 - External Power Connector Types

The inner and outer diameters of the mating plug are 2.0 mm and 5.5 mm respectively.

4.2 12 V Internal Power (J2201)

The Mercury+ PE3 base board base board can alternatively be powered through the internal power input connector J2201. The 12 V DC power source connected to J2201 must be filtered by external power circuitry. The internal power connector is not assembled by default.

Apply only 12 V DC to this connector.

Pin Number	Signal Name	Description
1	VCC_MAIN	12 V DC (nominal) input voltage
2	GND	Ground

Table 8: J2201 - Internal Power Connector

Table 9 lists the power connector type which can be optionally assembled on the Mercury+ PE3 base board.

Type	Manufacturer	Description	Assembly
0039290023	Molex	THT Connector Header 13 A	Option

Table 9: J2201 - Internal Power Connector Type

Warning!
Do not short circuit the 12 V power supply, and make sure the currents flowing through the pins of this connector do not exceed 11.0 A. Otherwise, the PCB may be damaged.

4.3 Fan Connector (J2202)

An external 12 V fan can be connected to J2202 connector.

Pin Number	Signal Name	Description
1	GND	Ground
2	VCC_MAIN	12 V DC (nominal) input voltage
3	SYSMON_TACHO	Connected to the System Monitor

Table 10: J2202 - Fan Connector

Type	Manufacturer	Assembly
61900311121	Würth Elektronik	Optional

Table 11: J2202 - Fan Connector Type

Table 12 shows an example of a mating part for the fan connector. This connector is without female crimp contacts or wires.

Type	Manufacturer
61900311621	Würth Elektronik

Table 12: Mating Part for the Fan Connector

4.4 I/O Voltage Selection (J2100)

The I/O voltage selection jumpers are used to configure the VCC_IO_A and VCC_IO_BC voltages that power the I/O banks of the SoC/FPGA device on the Mercury module. Refer to Section 5.5 for details.

4.5 Mercury Module Connector (J200/J201/J300)

A detailed pinout of the Mercury module connector can be found in the Mercury Master Pinout [9] and in the Mercury+ PE3 Base Board User Schematics [4].

Warning!

Only Enclustra Mercury FPGA/SoC modules should be inserted into the Mercury+ PE3 base board.

Warning!

The VCC_IO pins are directly connected to the FPGA/SoC device. Apply only compliant voltages to the VCC_IO pins; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE3 base board.

4.6 USB Type-A Host Connector (J600)

The Mercury+ PE3 base board is equipped with a USB Type-A USB SuperSpeed (3.2 Gen 1) host connector.

If the mounted Mercury module features a USB controller, the module's USB HighSpeed signals can be connected to J600 via a multiplexer. Details on USB HighSpeed connections on the board are available in Section 6.3.

The routing of the USB SuperSpeed signals depends on the MGT multiplexing configuration - refer to Section 6.2 for details.

The power and data signals on this connector are ESD-protected.

4.7 USB Type-C Connector (J602)

The USB Type-C connector has support for USB SuperSpeed (3.2 Gen 1), alternate mode DisplayPort and power delivery.

Name	Specification
USB datarate	USB 3.2 Gen 1 (1 lane @ 5 Gbit/s)
Direction	DRD (Dual Role Data, Host or Device)
Alternate Mode DisplayPort	
Direction	DFP_D (Downstream Facing Port, Video output)
Number of Lanes	1 (2 as an assembly option)
Power Delivery	
Type	DRP (Dual Role Power, Sink or Source)
Sink capabilities	5V/3A (15W), 12V/3A (36W)
Source capabilities	5V/3A (15W)

Table 13: J602 - USB Type-C Connector

The default assembly option of the Mercury+ PE3 base board supports one-lane DisplayPort. Two-lane DisplayPort is possible with a change of the assembly. The second DisplayPort lane is shared with the M.2 SATA/NVMe connector.

The high-speed routing of the USB Type-C connector J602 depends on the USB 2.0 switches U700 and U701. See Section 6.3 for further details.

USB SuperSpeed signals are routed to the USB Type-C multiplexer U707 which is controlled by the USB Type-C controller U804. The USB Type-C controller is also responsible for the USB power management.

4.8 Micro USB 2.0 Device Connector (J601)

The USB Micro-B connector on the board is connected to the FTDI device via a multiplexer. It can be used for UART, JTAG or SPI communication. Refer to Section 6.3.3 for details on the FTDI device. The power and data signals on this connector are ESD-protected.

4.9 Dual Gigabit Ethernet Port Eth0/Eth1 (J1500-A/J1500-B)

There are two 10/100/1000 Mbit Ethernet ports on the Mercury+ PE3 base board. The capability of the Ethernet interface depends on the connected Mercury module.

The RJ45 connector and the magnetics are equipped on the base board, while the Ethernet PHY is equipped on the Mercury module.

Each of the two RJ45 connectors can be used as 1 Gigabit Ethernet port or as 2 x 10/100 Mbit Ethernet ports, depending on the equipped Mercury module.

If one of the RJ45 connectors on the board is used for a dual Fast Ethernet implementation, an external RJ45 Y-adapter/splitter is required in order to convert the 4-pairs connection into 2 x 2-pairs connections.

4.10 SFP+ Connectors (J1701/J1702/J1703/J1704)

The capability of the SFP+ interface depends on the connected Mercury module as well as on the plugged SFP+ module.

The serial interface data and clock lines for each SFP+ channel are connected to separate I2C buses - the I2C bus structure is described in detail in Section 6.6.

The routing of SFP+ RX/TX signals depends on the MGT multiplexing configuration - refer to Section 6.2 for details. The SFP+ control and status signals (TXFAULT, TXDISABLE, RATESELECT, LOS) are connected to the on-board SFP+ I2C expander.

Table 14 lists the SFP+ connector and cage types used on the Mercury+ PE3 base board.

Part Type	Part Number	Manufacturer	Number of Parts Equipped
SFP+ connector	1888247-2	TE Connectivity	4
Quad SFP+ cage	U77-A461M-2081	Amphenol CS	1

Table 14: SFP+ Connectors and Quad SFP+ Cage Types

For details on connections to the SFP+ connectors, please refer to the Mercury+ PE3 Base Board User Schematics [4]. Note the assembly of SFP+ connector and SFP+ cage depends on the product model.

4.11 QSFP+ Connector (J1700)

The capability of the QSFP+ interface depends on the connected Mercury module as well as on the plugged QSFP+ module.

The serial interface data and clock lines are connected to the I2C bus - the I2C bus structure is described in detail in Section 6.6.

The routing of QSFP+ RX/TX signals depends on the MGT multiplexing configuration - refer to Section 6.2 for details. The QSFP+ control and status signals (MODPRSL, LPMODE) are connected to the on-board SFP+ I2C expander.

For details on connections to the QSFP+ connector, please refer to the Mercury+ PE3 Base Board User Schematics [4].

Table 15 lists the QSFP+ connector and cage types used on the Mercury+ PE3 base board.

Part Type	Part Number	Manufacturer
QSFP+ connector	FS1-R38-20A2-10	Amphenol CS
QSFP+ cage	U90-A111-1001	Amphenol CS

Table 15: QSFP+ Connector and Cage Type

4.12 HDMI Connector (J1501)

The Mercury+ PE3 base board supports HDMI 1.4b and 2.0b output signals. The signals available on this connector are routed via HDMI retimer U1500 to the MGT multiplexing circuit - refer to Section 6.2 for details.

I2C_MGMT_CH0_LS is used to configure the HDMI retimer (U1500). I2C_USER_CH7 is level shifted to 5V via U1500 and connected to the HDMI connector. Refer to Section 6.6 for detailed information about I2C connection.

The pinout on the HDMI connector corresponds to the HDMI standard. In order to transmit video signals through the links, FPGA support is required (video protocol implementation).

This interface is protected against electrostatic discharge (ESD) by using TVS diodes.

4.13 Firefly Connector (J1401/J1402)

By default, the Mercury+ PE3 base board supports ECUO, ETUO and ECUE Firefly modules with 4 RX/TX pairs and up to 10 Gbit/s datarate.

Four additional FPGA I/O pairs are connected to the reserved (RSVD) pins of the Firefly connector (J1401). These additional I/Os FF_DIO<0-3>_P/N are referenced to VCC_IO_A. Please refer to the Mercury Master Pinout [9] or the Mercury+ PE3 Base Board User Schematics [4], for details on these connections.

The Firefly TX and RX signals are routed to the MGT multiplexing circuit. Refer to Section 6.2 for details on MGT multiplexing options.

Warning!

IOs FF_DIO<0-3>_P/N are connected directly to the FPGA/SoC device.

The IO voltage of FF_DIO<0-3>_P/N must not exceed VCC_IO_A, otherwise the mounted Mercury FPGA/SoC module may be damaged.

4.14 M.2 Socket (J1400)

The Mercury+ PE3 base board is equipped with a M.2 socket, which can be connected an MGT transceiver via MGT multiplexers - see Section 6.2 for details. Table 16 lists the specification of supported SSDs. In addition, the module used in combination with the Mercury+ PE3 base board must also support the used SSD.

Name	Specification
Protocol	SATA or NVMe
Key	M or B&M Key
Length	2242, 2260 or 2280

Table 16: J1400 - M.2 specification

The MGT transceiver may optionally be connected to an additional DisplayPort lane, instead of the M.2 socket. By default, the M.2 socket is connected to the MGT (while DisplayPort supports a single lane), and as an assembly option M.2 socket may remain unused (while DisplayPort can use two lanes).

The polarity of M2_RX0 was chosen to fulfill SATA standard. For PCIe support lane polarity reversal must be activated.

4.15 FMC Connector (J1600)

This connector allows the extension of the Mercury+ PE3 base board with other FMC (FPGA Mezzanine Card) modules (Enclustra or third-party).

For details on the pinout of the FMC HPC (High Pin Count), please refer to the VITA 57 FMC specification.

Table 17 describes the FMC connector present on the Mercury+ PE3 base board.

Warning!

The FMC I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE3 base board.

FMC Connector Name	Connector Type	Manufacturer
FMC HPC connector	ASP-134486-01	Samtec

Table 17: J1600 - FMC HPC Connector Type

Table 18 includes information related to the total number of I/Os available on the FMC connector.

Note that certain user-defined I/Os or multi-gigabit transceivers and clocks are supported only in combination with Mercury+ modules, which are equipped with a third connector (module connector C).

Signal Name	FMC Pin Type	Single Ended	Pairs	Module Connector
FMC_DP<0-7>_C2M_P/N	DP C2M	-	8	Depends on multiplexing - see Figure 19
FMC_DP<0-7>_M2C_P/N	DP M2C	-	8	Depends on multiplexing - see Figure 19
FMC_GCLK0_M2C_P/N	GBTCLK M2C	-	1	Depends on multiplexing - see Figure 18
FMC_GCLK1_M2C_P/N	GBTCLK M2C	-	1	Depends on multiplexing - see Figure 18
FMC_CLK<2-3>_BIDIR_P/N	CLK BIDIR	-	2	C Only as an assembly option available
FMC_LA<...>CC_P/N	LA CC	8	4	B
FMC_LA<...>_P/N	LA	60	30	B
FMC_CLK<...>_M2C_P/N	CLK M2C	-	2	B
FMC_HA<...>_CC_P/N	HA CC	6	3	C
FMC_HA<...>_P/N	HA	42	21	C
FMC_HB<...>_CC_P/N	HB CC	6	3	C Only as an assembly option available
FMC_HB<01-04>_P/N	HB	8	4	C
FMC_HB<05...19>_P/N	HB (non-CC)	26	13	C Only as an assembly option available

Table 18: Available I/Os on the FMC Connector

The signal names on the module connectors indicate to which pins of the FMC HPC connector they are routed to.

Both GBT M2C clock pairs are AC coupled. Pins with the name MGT_<T/R>X_<>_FMC_HB<...>_P/N on module connector C are only available as an assembly option.

The FMC I2C interface is connected to the User I2C interface channel 6 (I2C_USER_CH6_SDA/SCL_FPGA). Details on I2C routing can be found in Section 6.6.

Detailed information about the routing of the FMC clock and the FMC data can be found in section 6.1 and section 6.2, respectively.

Please refer to the Mercury Master Pinout [9] and the Mercury+ PE3 Base Board User Schematics [4], for details on FMC connectivity.

4.16 PCIe ×8 Edge Connector (J1200)

The Mercury+ PE3 base board has a PCIe ×8 edge connector, which allows using the board with standard CPU motherboards having a PCIe slot.

The routing between the PCIe edge connector and the Mercury module depends on the MGT multiplexer circuit configuration - see Section 6.2 for details. The connection of the PCIe signals to the edge connector is made via PCIe redrivers.

The PCIe reference clock can either be forwarded to the Mercury module or it can be used as an input for the clock generator 6.1.2. The routing depends on the settings of MGT multiplexers 0 and 1 (U1000 and U1001).

The PCIe ×8 edge connector can be used in two hardware configurations:

1. PCIe endpoint standard configuration - ×1, ×2, ×4 or ×8 PCIe communication between the Mercury module and a PCIe host/motherboard. In this configuration:
   - The Mercury module device is configured as a PCIe endpoint
   - It complies with the PCIe standard
   - The Mercury+ PE3 base board is powered over PCIe (see Section 5.2.1)
   - The PCIe reset signal (PCIE_PERST#) is connected through the system controller to SIO0_PERST# by default (routed to Mercury connector pin A-104 to be used as PERST# signal for the PCIe endpoint implemented on the module)
   - The transceiver data signals are routed through the MGT multiplexers (see Section 6.2)
   - The PCIe reference clock is provided either via clock generator and MGT multiplexers or directly via MGT multiplexer (see Sections 6.2 and 6.1).
2. PCIe non-standard configuration - usage of the Mercury+ PE3 base board as standalone board, and connection to a custom board via the PCIe ×8 edge connector. In this configuration:
   - The Mercury module device acts as a host (note that this is not a standard PCIe root complex configuration)
   - The Mercury+ PE3 base board provides a 12 V power supply connection to the custom board. The EIO_DETECT# (PCIe edge connector, pin B-8) signal must be driven low from the custom board. This will drive the signal EIO_PWR_EN#. As an alternative the signal EIO_PWR_EN# can be driven directly by the system controller.
     Note that the 3.3 V power connection is not provided by the Mercury+ PE3 base board and has to be generated on the external custom board if required.
   - The Mercury+ PE3 base board provides a USB connection to the custom board. R702 and R704 must be equipped to enable this connection.
   - The Mercury+ PE3 base board provides four system controller GPIO signals on the edge connector. These can be driven by the system controller.
   - The USB and GPIO signals mentioned above are mapped to JTAG, reserved and special function pins of the PCIe edge connector (therefore not compliant to the PCIe standard pinout).

4.17 microSD Card Slot (J1403)

The enclosure of J1403 is connected to GND.

The microSD card signals are connected via a multiplexer with a built-in level shifter to the Mercury module SDIO signals.

4.18 Anios I/O Connector (J2000)

The Anios I/O connector can be used for user applications: the connector provides 24 user I/Os, a differential clock connection, connectivity to the I2C User bus, and power supply connections. The clock, data and I2C signals are routed to the module connector B - for details, refer to the Mercury+ PE3 Base Board User Schematics [4].

Warning!

The Anios I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE3 base board.

4.19 Digital I/O Connectors (J1800/J1801/J1901/J1902)

There are four digital I/O connectors equipped on the Mercury+ PE3 base board. Two of them are used for clock input and output signals and the other two are used for digital data input and output signals.

Table 19 lists the type of digital I/O connectors used on the Mercury+ PE3 base board.

RF Connector Name	Connector Type	Manufacturer
Mini RF Header	1909763-1	TE Connectivity

Table 19: Clock and Digital Data RF Connector Type

Details about clock connections can be found in section 6.1

Table 20 and Figure 10 illustrate the connections for the digital data input and output lines.

Module Connector Pin	Module Connector Signal	Connectivity
A-76	DII_LED#	Digital input (shared with DII user LED)
A-78	DIO_LED#	Digital output (shared with DIO user LED)

Table 20: Digital I/O Connectivity

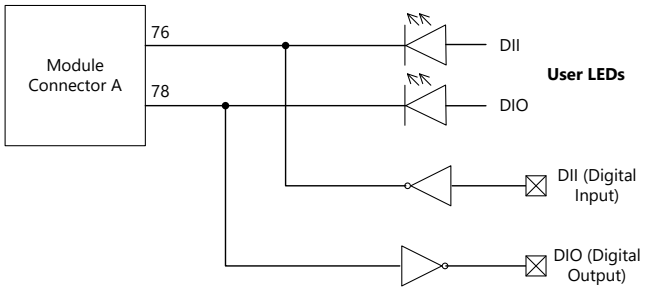


Figure 10: Digital I/O Connectivity

4.20 Battery Holder (J2101)

A 3 V lithium battery (CR1220) can be installed for buffering the real-time clock on the connected Mercury FPGA/SoC module. The battery is not included.

Alternatively, the VCC_BAT_IN power signal can be driven via pin 6 of connector J2001. Refer to Section 4.22 for details.

Type	Manufacturer
BC501SM	Memory Protection Devices

Table 21: J2101 - Battery Holder Type

Warning!

There is a danger of explosion if the battery is replaced incorrectly - only replace the battery with the same or equivalent type recommended by Enclustra.

Used batteries should be disposed of according to the manufacturer's instructions.

4.21 JTAG Connector (J2003)

The JTAG routing depends on the presence of a FMC Mezzanine card. If a FMC card is mounted on the Mercury+ PE3 base board, the JTAG is routed through the mounted FPGA/SoC module and the FMC card. Otherwise, the JTAG loop includes only the FPGA/SoC module.

Figure 11 describes the routing of the JTAG signals.

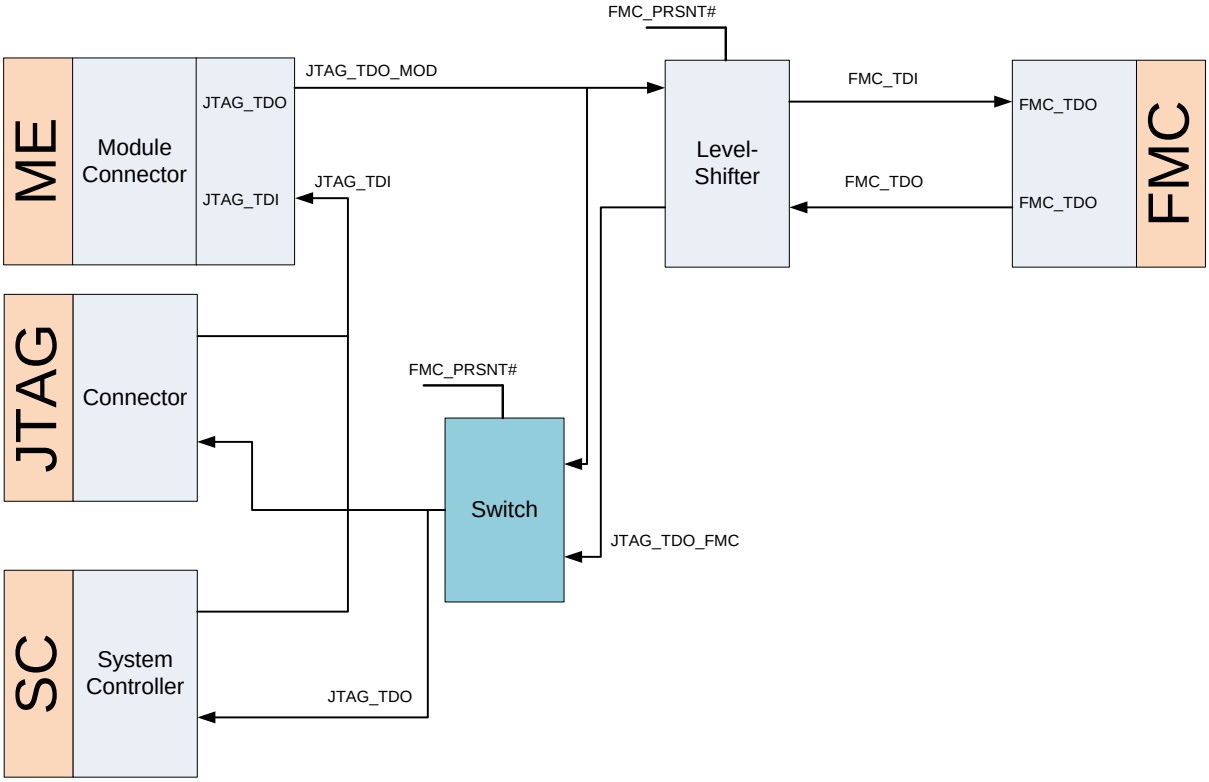


Figure 11: JTAG Routing

Pin Number	Connection	Series Resistor
1	JTAG_TCK	22 Ω
2	JTAG_PRSNT#	1 kΩ
3	JTAG_TDO	100 Ω
4	VCC_IO_A	-
5	JTAG_TMS	100 Ω
6	SRST#_RDY	100 Ω
7, 8	Not connected	-
9	JTAG_TDI	100 Ω
10	GND	-

Table 22: J2003 - FPGA JTAG Connector

JTAG_PRSNT# is used to determine if an external JTAG adapter is connected; the external adapter should tie this signal to GND when the cable is plugged in.

Warning!

The JTAG pins are connected to the FPGA/SoC device via small-value series resistors. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device. Any other voltages may damage the equipped FPGA/SoC device as well as other devices on the module or Mercury+ PE3 base board.

The JTAG connector available on the Mercury+ PE3 base board can be used in combination with Xilinx Platform Cable USB or Intel USB-Blaster download cable. For Xilinx JTAG connection, the flying wire adapter must be used.

For Intel JTAG connection, the pinout matches the Intel USB-Blaster pinout. The download cable can be connected directly to the on-board JTAG connector.

4.21.1 Xilinx JTAG over System Controller

The system controller includes built-in Xilinx JTAG programmer functionality, making it possible to use a USB connection for JTAG debugging. It is fully supported by the Xilinx tools.

The following steps need to be taken in order to use the Xilinx JTAG:

- Set the FTDI device in Xilinx JTAG mode using the Enclustra Module Configuration Tool (MCT) [11].
- Set the ScMode0 register to 0 (refer to Section 6.5)
- Set the USB_SEL signal so that the currently used USB connector is routed to the FTDI device (refer to Section 6.5)

Do not activate the Xilinx JTAG function while a JTAG adapter is plugged to the JTAG header.

4.21.2 Altera JTAG over System Controller

Currently, the built-in Altera JTAG functionality is not supported by the system controller.

4.22 Control Connector (J2001)

The control connector is used mainly for control and monitoring purposes. A 2x10 pin header connector of type *WR-PHD Dual Pin Header* by *WE* is used. Many control functions are affected by the signals connected to this connector. The power supply outputs (Pin 1 to 4) are intended for monitoring of the supply voltages. It is recommended to not exceed a current of 0.5 A on these pins. Detailed information can be found in table 23.

Pin Number	Signal Name	Description	Function
1	VCC_MAIN	12 V DC main voltage	Supply output / Monitor
2	GND	Ground	-
3	VCC_5V	5 V DC converter output	Supply output / Monitor
4	VCC_3V3_AUX	3.3 V DC Auxiliary	Supply output / Monitor

Continued on next page...

Pin Number	Signal Name	Description	Function
5	UART_RX_LS	3.3V level-shifted UART_RX	Control / Monitor
6	VCC_BAT_IN	External connection for battery supply	Supply input / Monitor
7	UART_TX_LS	3.3V level-shifted UART_TX	Control / Monitor
8	PWR_GOOD_IO	Power good status	Monitor
9	PWR_BTN#	External connection for power button, active-low	Control
10	PWR_EN	Power enable signal. Can be pulled low to disable most of the power converters on module and base board	Control / Monitor
11	GND	Ground	-
12	FTDI_BDBUS7_SCJTAGEN	Reserved for internal use	-
13	I2C_MGMT_SDA_LS	3.3V level-shifted I2C_MGMT_SDA	Control / Monitor
14	FTDI_BDBUS0_SCTCK_TXD	Reserved for internal use	-
15	I2C_MGMT_SCL_LS	3.3V level-shifted I2C_MGMT_SCL	Control / Monitor
16	FTDI_BDBUS1_SCTDI_RXD	Reserved for internal use	-
17	POR#_LOAD#_LS	3.3V level-shifted external connection for power-on reset, active-low	Control
18	FTDI_BDBUS2_SCTDO	Reserved for internal use	-
19	FPGA_DONE_LS	3.3V level-shifted FPGA configuration done status	Monitor
20	FTDI_BDBUS3_SCTMS	Reserved for internal use	-

Table 23: J2001 - Control Connector

5 Power

5.1 Power Generation Overview

The power generation is shared between the Mercury+ PE3 base board and the Mercury module. Power input can be provided to the base board in different ways (section 5.2) and shall provide 12 V to VCC_MAIN. The main power is used on the base board to create the VCC_5V, VCC_3V3 and VCC_3V3_AUX rails. VCC_MAIN is forwarded to the Mercury module as well. On the module, a separate 3.3 V rail (VCC_3V3_MOD) is generated. The voltages VCC_OUT_A, VCC_OUT_B and VCC_OUT_C are generated on the module from VCC_3V3_MOD. VCC_OUT_A, VCC_OUT_B and VCC_3V3_MOD are transmitted back to the base board, where VCC_3V3_MOD is used to generate the VCC_1V2 and VCC_1V8 voltages. The I/O Voltage for the Mercury module can finally be set to different generated voltages. This is done on the base board via jumper selection (section 5.5). An additional voltage input (VCC_FMC_VIOB) comes from the FMC card. Power generation is visualized in figure 12.

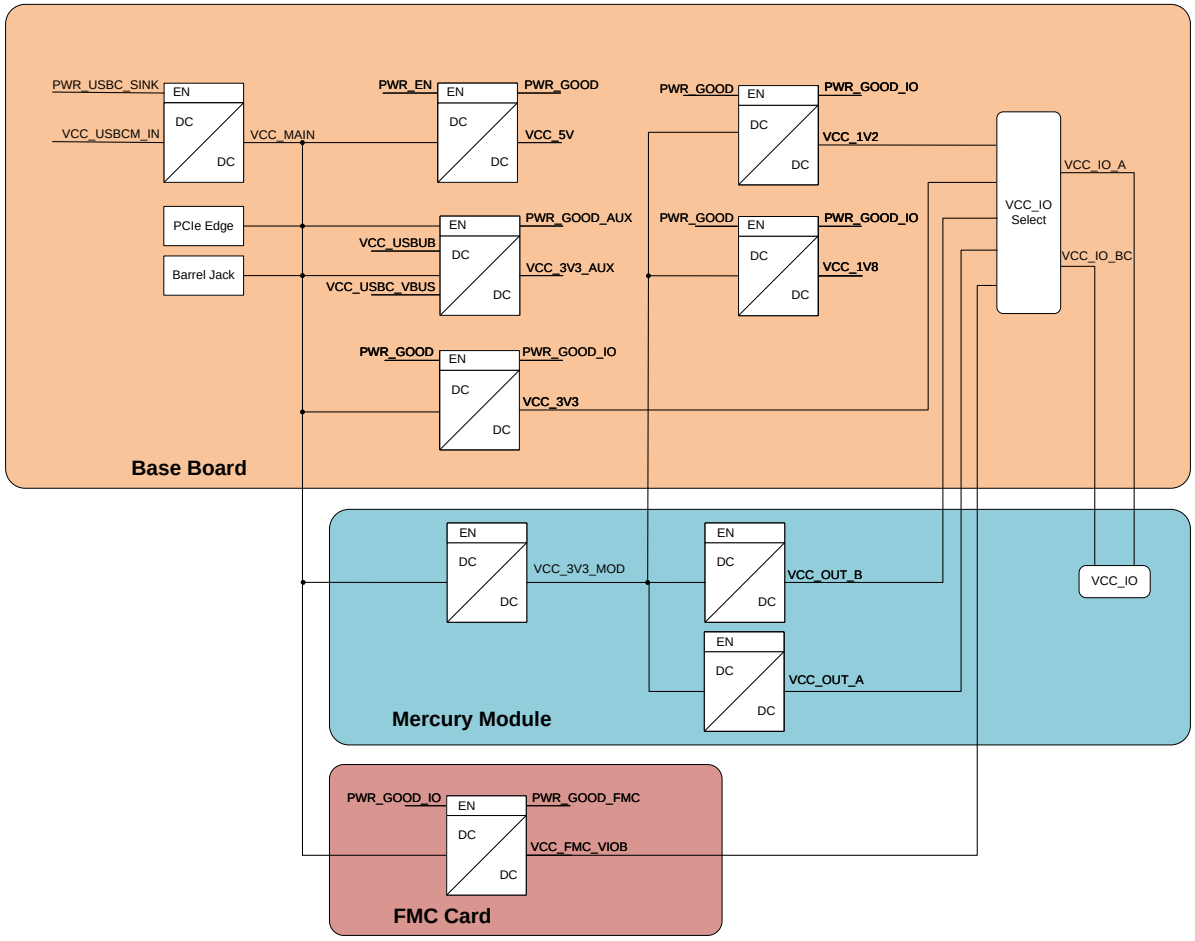


Figure 12: Power Generation Overview

Table 24 describes the power supplies available on the base board, together with current limitation and power sequence. As soon as the origin voltage is applied an the enable signal given, the voltage supply will start up. When startup is complete, the power good signal will be issued.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Origin	Enable Signal	Power Good Signal
VCC_MAIN	12.0 V	3.5 A	VCC_USBCM_IN[1]	PWR_USBC_SINK	PWR_GOOD_USBCM
VCC_5V	5.0 V	6 A	VCC_MAIN	PWR_EN	PWR_GOOD
VCC_3V3	3.3 V	6 A	VCC_MAIN	PWR_GOOD	PWR_GOOD_IO
VCC_1V8	1.8 V	2 A	VCC_3V3_MOD	PWR_GOOD	PWR_GOOD_IO
VCC_1V2	1.2 V	2 A	VCC_3V3_MOD	PWR_GOOD	PWR_GOOD_IO
VCC_3V3_AUX	3.3 V	3 A	VCC_MAIN VCC_USBUB VCC_USBC_VBUS	N/A	PWR_GOOD_AUX

Table 24: Generated Power Supplies

Warning!

The maximum available output current for each voltage supply depends on your design. Make sure that the Mercury module I/O banks and the FMC cards do not draw more current than available on the output of the DC-DC converter.

5.2 Power Input

The Mercury+ PE3 base board can be powered using one of the power input sources listed below:

- External power connection through J2200 barrel jack connector
- Internal power connection through J2201 connector
- PCIe power connection
- Power via USB Type-C

5.2.1 Power over PCIe (J1200)

By default, the Mercury+ PE3 base board is powered over the external (J2200) or internal (J2201) power connection. If a PCIe connection over the edge connector is detected the Mercury+ PE3 base board is powered over PCIe via the edge connector.

Warning!

It is possible to power the PCIe power supply pins by the on-board power supply. Drive EIO_DETECT# signal low to obtain PCIe power output - note that this does not correspond to the PCIe specification. Refer to Section 4.16 for more information.

When using power over PCIe, make sure that the power over USB is disabled; please refer to Section 5.2.2 for details.

[1]This power origin and the corresponding sequencing signals are only used when power over USB Type-C is enabled. In other cases, VCC_MAIN is provided via PCIe or via external or internal connectors.

5.2.2 Power over USB Type-C (J602)

The USB Type-C port on the Mercury+ PE3 base board supports Dual Role Power (DRP), which means the port can act as a power source or power sink. Therefore the Mercury+ PE3 base board can power an external device connected via USB Type-C or it can be powered via USB Type-C.

The PE3 USB Type-C Application Note [13] descibes the required configuration to use Power Delivery functionality of the USB Type-C port.

5.3 Power Control

Power control is enabled and disabled by the PWR_ON# signal, determined by the position of the DIP switch CFG A 4. Table 25 describes the power control configuration; the factory default is marked in bold.

DIP Switch CFG A 4	PWR_ON#	Effect
OFF	1	Power control is enabled
ON	**0**	**Power control is disabled**

Table 25: Power Control Switch Configuration

If power control is disabled, the Mercury+ PE3 base board and the mounted module are powered as soon as power is applied through external or internal power connectors.

If power control is enabled, the Mercury module is not powered, even when power is applied to the external power input. By pressing the power button (PWR) for a short time, the power is turned on. Power can be turned off again by pressing the power button for a configurable time. Power can also be turned on and off by writing a system controller register - see Section 6.11 for more information.

Power control is not available when power over USB Type-C or PCIe is active.

5.4 Enable and Reset Control

Due to the number of power-supplies and sub systems, power enable and system reset signals have many dependencies. Table 26 describes all control signal dependencies

Signal	Signal Type	Origin	Dependencies	Comment
VCC_MAIN	Supply Voltage	Base board	Power input, Power control	
VCC_3V3_MOD	Supply Voltage	Module	VCC_MAIN	
PWR_EN	Enable	Base board	VCC_3V3_MOD, Control connector	General Power Enable Signal
PWR_GOOD	Enable, Power Good	Module, Base Board	PWR_EN, VCC_5V, VCC_3V3_MOD, Module supplies	Power Good core supplies
PWR_GOOD_IO	Enable, Power Good	Base board	VCC_1V2, VCC_1V8, VCC_3V3, PWR_GOOD, FMC connector	Power Good I/Os
POR#_LOAD#_CT	Reset	Base board	PWR_GOOD_IO, POR button, PWR_GOOD_FMC	
POR#_LOAD#	Reset	Base board	POR#_LOAD#_CT, Control connector, System controller	Module Power-on-reset
SRST#_RDY#	Reset	Base board	JTAG, System controller, SRST button	Module soft-reset or configuration-delay signal

Table 26: Power Control Switch Configuration

All enable and reset signals in Table 26 are open-drain signals.

The power enable signal, PWR_EN, may be used to shut down the DC-DC converters on the Mercury module - please refer to the module's user manual for details on power generation.

5.5 I/O Voltage Selection

The I/O voltage selection jumpers are used to configure VCC_IO_A and VCC_IO_BC voltages that power the I/O banks of the SoC/FPGA device on the Mercury module as well as the I/O voltage VCC_FMC_ADJ for the FMC card.

The VCC_IO voltages are configurable by applying the required voltage from VCC_OUT_A, VCC_OUT_B, VCC_1V2 or VCC_3V3 pins. This can be done by setting the I/O selection jumpers accordingly. VCC_FMC_VIOB can also be connected to SoC/FPGA I/O banks, but wire jumpers are needed to realize this connection.

Table 27 describes the usage of jumpers. Please note the following:

- VCC_OUT_A and VCC_OUT_B are supply outputs from the Mercury module. The value of these voltages depend on the mounted Mercury module (Refer to the "Voltage Supply Outputs" Section in the Mercury module user manual).
- VCC_FMC_VIOB is a supply output from the FMC card.
- Only one source for each I/O voltage VCC_IO_A or VCC_IO_BC is allowed.
- The factory default jumper settings are 3-5, 6-8. As a consequence of these settings, no voltage is applied to the Mercury module connector, therefore it prevents the module from booting. PWGD LED will not be lit.

Make sure that the jumper configuration chosen does not short power nets together.
To provide power to the VCC_IO_A, VCC_IO_BC pins, two jumpers are included in the product deliverables. Please note that not all combinations can be realized with jumpers; wire jumpers can be used instead when required.

Jumper Position	VCC_1V2	VCC_OUT_A	VCC_OUT_B	VCC_3V3
VCC_IO_A	-	10-12	8-10	9-10
VCC_IO_BC	3-4	1-3	5-6	5-7

Table 27: IO Voltage - Jumper Settings

Warning!

Do not merge power pins. Merging power pins can damage the Mercury module or FMC card.

Warning!

Use only VCC_IO_A and VCC_IO_BC voltages compliant with the equipped Mercury module; any other voltages may damage the equipped Mercury module, as well as other devices connected to Mercury+ PE3 base board.

Figure 13 shows the pin numbering for the connector J2100. Figure 14 provides one configuration example.

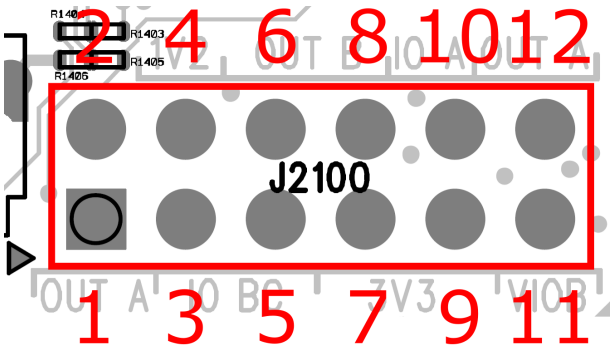
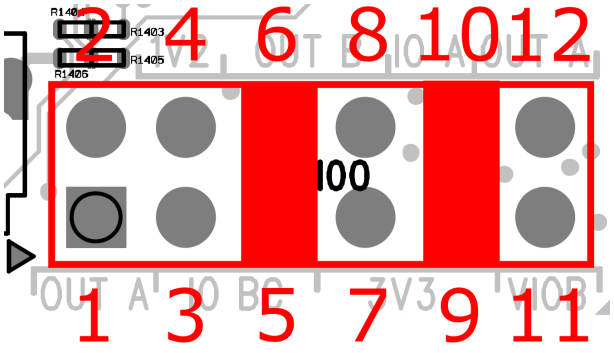


Figure 13: IO Voltage Selection - Pin Numbering



Example:
VCC_IO_A = VCC_3V3
VCC_IO_BC = VCC_OUT_B

Figure 14: IO Voltage Selection - Configuration Example

6 Board Function

6.1 Clock Architecture

The Mercury+ PE3 base board provides the user with a diversity of clock configuration options. The board is equipped with a clock generator and a number of reference clocks from different sources can be supplied to the module. The Mercury+ PE3 base board has a crystal oscilator and can take clocks from external connectors like FMC and PCIe.

6.1.1 Module Clocks

Each MGT bank on the module connector has two reference clocks for a total of ten clocks. Graphic 15 shows the clock connection to each bank. The clocks can be supplied from different sources, which is described in the following sections.

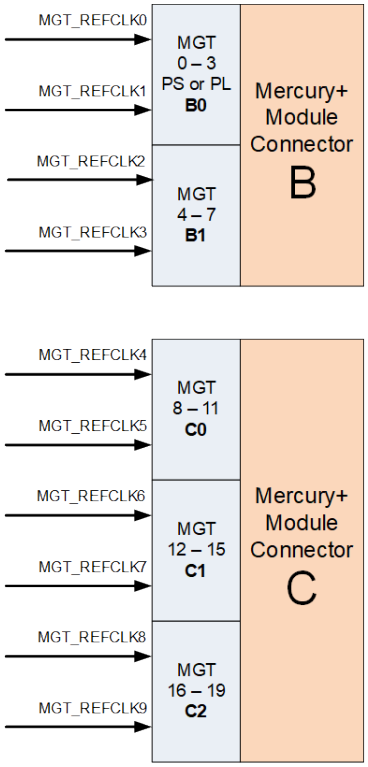


Figure 15: Module Clocks

6.1.2 Clock Generator

The Mercury+ PE3 base board features a clock generator circuit addressable and configurable via I2C. The clock generator has the following possibilities for input clocks:

- On XA/XB inputs: 25 MHz clock from a crystal (Y1803)
- On CLKIN_2 inputs: the PCIe reference clock routed via the MGT multiplexer circuit
- On CLKIN_3 inputs: the clock inputs from the RF connector (micro-coaxial connection)

Alternatively, a user oscillator (Y1801) with another frequency can be used as reference - this part is not equipped by default on the board. The clock from this oscillator can be connected to CLKIN_2 or CLKIN_3.

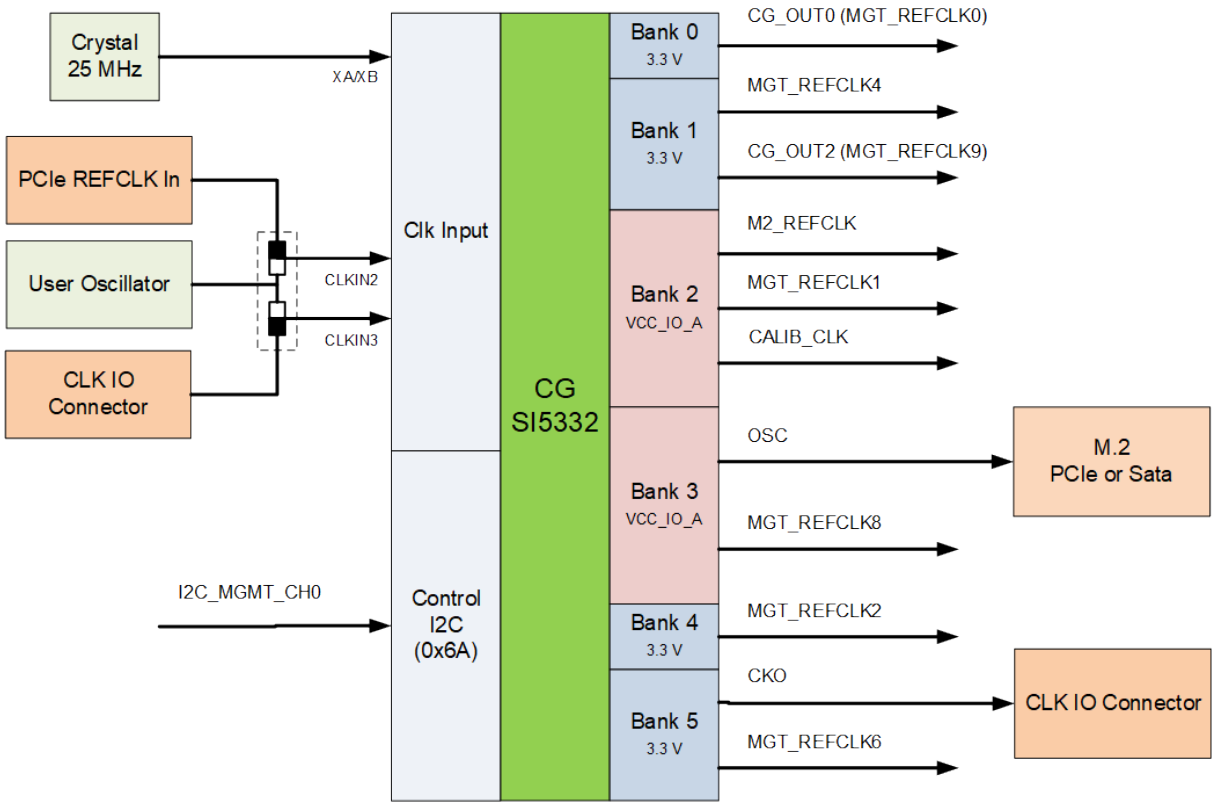


Figure 16: Clock generator

The clock generator has to be configured at power-up via I2C by the Mercury module or by another I2C master. By default, the PCIe reference clock is routed to the differential inputs CLKIN_2_P and CLKIN_2_N of the clock generator circuit via a multiplexer - see Figure 17. The device also provides the option of storing a user-defined clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up. The NVM is a one-time programmable (OTP) memory.

The SI5332A device can be reconfigured to desired functionality via the I2C interface. ClockBuilder ™ Desktop Software is a tool provided by Silicon Labs, which allows the user to specify several settings, such as the input clock pins and clock frequency, the output clock frequencies and phase shifts. The I2C Application Note [10] describes how the clock generator can be programmed with a new config via I2C.

For details on features and configuration, refer to the SI5332A datasheet.

Warning!
Writing the contents of the NVM OTP configuration memory voids the board warranty.

Type	Manufacturer
SI5332A-D-GM3	Silicon Labs

Table 28: Clock Generator Type

6.1.3 PCIe Clocks

For the PCIe clock are three posibilities:

- Route the clock coming from the PCIe connector directly to the MGT_REFCLK0 pin on the module connector.
- Route the PCIe clock to an input of the clock generator and output a clock dependend on the PCIe clock to any of reference clock outputs.
- Generate a clock that is independent to the PCIe clock on any of the reference clock outputs.

To use the PCIe clock, the clock multiplexer and the clock generator need to be configured. The Mercury PE3 Multiplexing App Note [12] describes the configuration of the clock multiplexer and the section 6.1.2 descibes the clock generator.

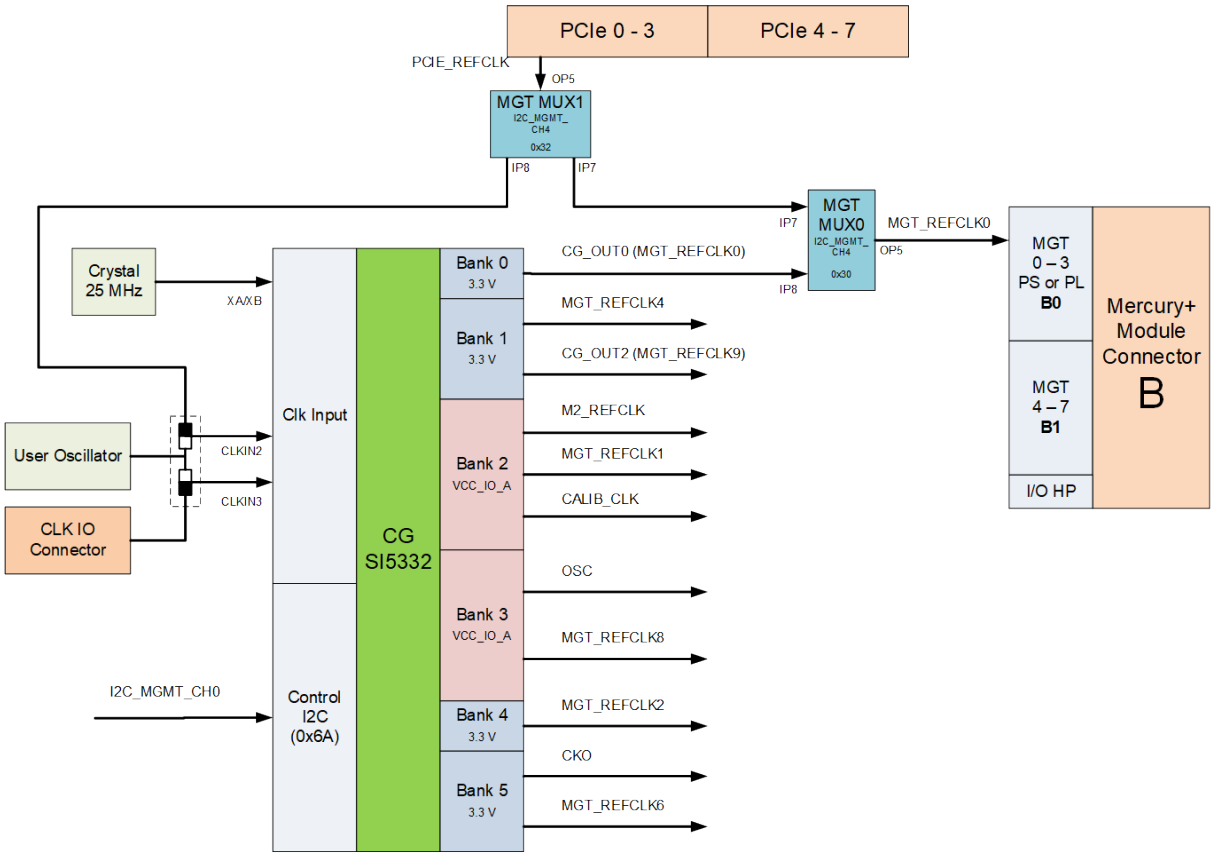


Figure 17: PCIe Clock

6.1.4 FMC Clocks

A clock can be provided by the FMC connector and routed to different reference clock inputs of the module. See figure 18 for the different routing options and connections. The Mercury PE3 Multiplexing App Note [12] describes the configuration of the clock multiplexer.

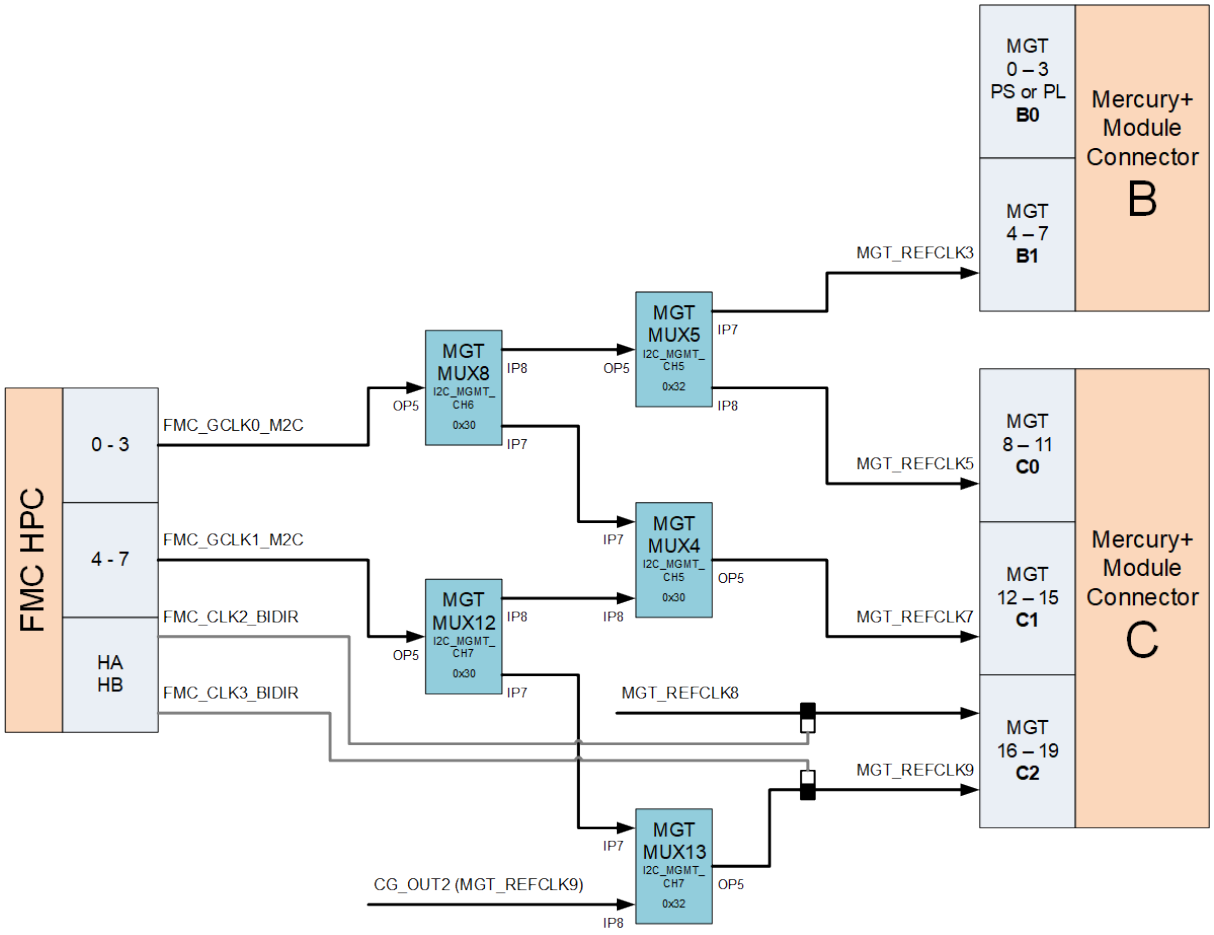


Figure 18: FMC Clock

There is also an assembly option to use two additional clocks from the FMC connector.

For further information please refer to the Mercury+ PE3 Base Board User Schematics [4].

6.2 MGT Multiplexers

Depending on the equipped Mercury module, Mercury+ PE3 base board supports up to twenty MGT connections to nine different MGT interfaces. To allow flexible routing between the Mercury module and the MGT interfaces, the Mercury+ PE3 base board includes a complex MGT multiplexer circuit. To achieve the desired routing through the MGT multiplexer circuit, all the MGT multiplexer devices must be configured accordingly.

Figure 19 shows an overview of the MGT multiplexing circuit. The clock connections described in section 6.1 are realized using the same MGT multiplexing devices. Each of the five MGT banks (2 on Module connector B and 3 on Module connetor C) contain four TX/RX pairs.

Nearly all MGT interfaces can be routed to most MGT blocks. An exception is the selection between M.2 TX data, and the second DisplayPort data path for USB Type-C alternative mode. To use M.2, resistors R972 and R974 must be equipped - this is the default assembly. To support DisplayPort with two lanes, resistors R973 and R975 must be equipped - this is an assembly option.

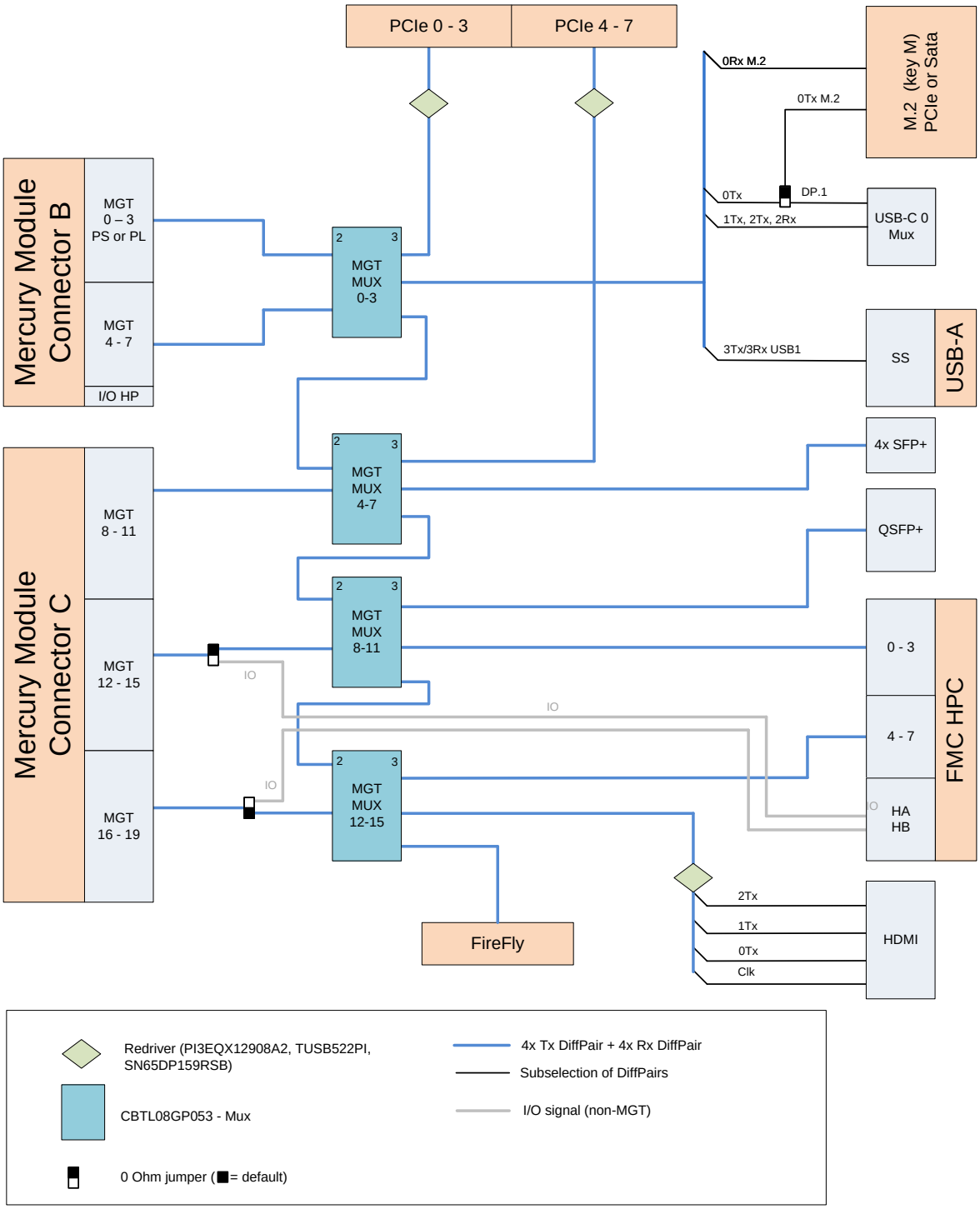


Figure 19: MGT Multiplexing Overview

6.3 USB

The Mercury+ PE3 base board has three USB connectors and supports modules with different USB functions. For debugging purposes, the Mercury+ PE3 base board has an FTDI chip, which supports different functions like UART or JTAG. Depending on the use case, the USB connectors can be routed to different USB sources via multiplexer. The USB capabilietes depend on the module connected to the Mercury+ PE3 base board. Except for the FTDI chip, the Mercury+ PE3 base board passes the USB signals to the module. The PHYs or MGTs have to be available on the module.

The USB connectors of the Mercury+ PE3 base board have the following purpose:

- **USB Type-A connector**
  The USB Type-A connector is a host connector and supports USB HighSpeed (2.0) and SuperSpeed (3.2 Gen 1) datarates.
- **USB Type-C connector**
  The USB Type-C connector can be used for device and host connections and supports USB HighSpeed (2.0) and SuperSpeed (3.2 Gen 1) datarates. In addition Power Delivery and DisplayPort alternate mode is supported.
  The connector can either be used for a connection with the module or be connectoed to the FTDI chip on the Mercury+ PE3 base board.
- **USB Micro-B connector**
  The USB Micro-B header can only be used with the FTDI chip on the Mercury+ PE3 base board.

The module connector on the Mercury+ PE3 base board has the connections to support the following USB functions:

- **2x USB HighSpeed (2.0) PHYs**
  The two USB HighSpeed (2.0) PHYs of a connected module can be used with the USB Type-A and USB Type-C connector.
- **2x USB SuperSpeed (3.2 Gen 1) MGTs**
  Two MGT pairs on module connector B can be used for USB SuperSpeed (3.2 Gen 1) and be connected to the USB Type-A and USB Type-C connector.
- **FX3**
  The FX3 signals on module connector A can be routed to the USB Type-C connector.

To use any of these USB functions, the multiplexing circuit on the Mercury+ PE3 base board needs to be configured. The muliplexer nets for USB HighSpeed and SuperSpeed are seperate and need to be configured individually.

6.3.1 USB HighSpeed (2.0) Multiplexing

The Mercury+ PE3 base board has multiplexers to connect the USB interfaces to different sources. The multiplexer for the USB HighSpeed (2.0) connections are configured with DIP switches. Graphic 20 shows the multiplexing circuit and table 29 lists the different configurations.

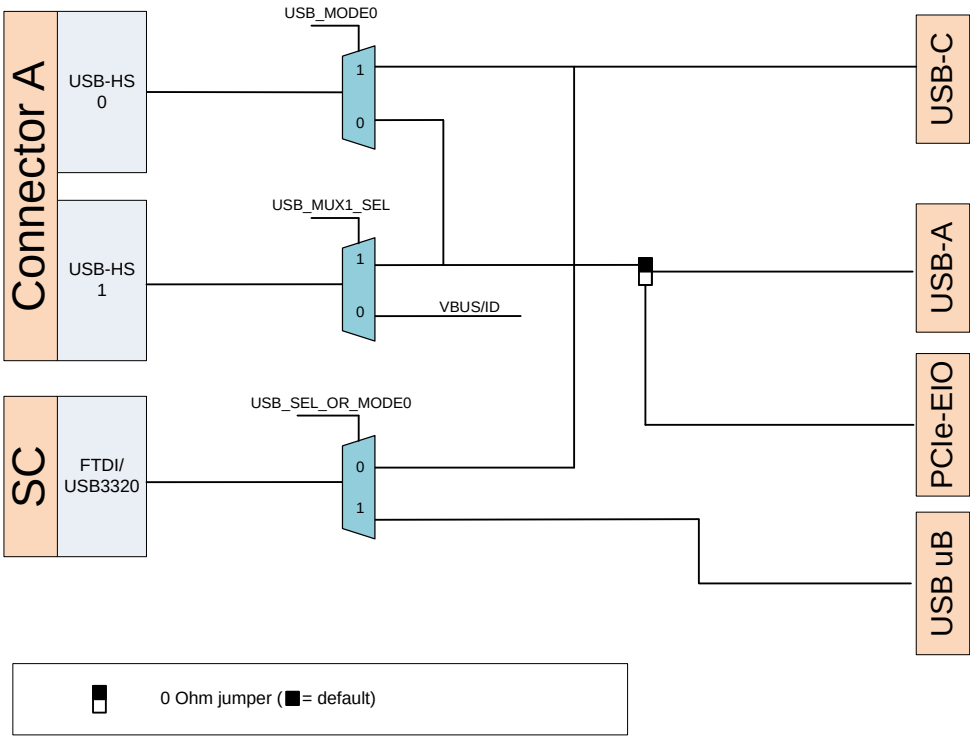


Figure 20: USB HighSpeed (2.0) Connections Overview

The USB Type-C connector can be connected with the first USB HighSpeed PHY (HS0). The USB Type-A connector can be connected with both USB HighSpeed PHYs. In case USB SuperSpeed is used, only the second PHY (HS1) can be used for the USB Type-A connector.

The FTDI chip can either be used with the USB Micro-B or the USB Type-C connector.

CFG B 1 USB_MODE0	CFG B 2 USB_MODE1	CFG B 3 USB_SEL	USB-HS0 Pins A-131/A-133	USB-HS1 Pins A-127/A-129	FTDI
0 (ON)	X	0 (ON)	USB Type-A	VBUS/ID	USB Type-C
0 (ON)	X	1 (OFF)	USB Type-A	VBUS/ID	USB Micro-B
1 (OFF)	0 (ON)	X	USB Type-C	VBUS/ID	USB Micro-B
1 (OFF)	1 (OFF)	X	USB Type-C	USB Type-A	USB Micro-B

Table 29: USB High-Speed Connection Table

6.3.2 USB SuperSpeed (3.2 Gen 1) Multiplexing

The USB SuperSpeed (3.2 Gen 1) connections are routed via the MGT multiplexers. The configuration of the MGT multiplexers is described in section 6.2. A SuperSpeed connection uses the signals for USB HighSpeed and SuperSpeed, therefore the USB HighSpeed multiplexer need to be configured as well. One RX/TX pair on the first MGT bank of the Mercury Module connector B can be connected to the USB Type-C connector and another pair can be connected to the USB Type-A port.

The configuration of the USB Type-C controller chip of the Mercury+ PE3 base board is described in the PE3 USB Type-C Application Note [13]

The Mercury+ PE3 base board supports also the USB SuperSpeed connection for a module with an FX3. The FX3 can only be used with the USB Type-C connector. The required USB HighSpeed configuration for the FX3 is CFGB1 OFF and CFGB2 ON.

6.3.3 USB 2.0 Device Controller (FTDI)

The FTDI FT2232HQ USB 2.0 device controller present on the Mercury+ PE3 base board can be used to easily implement a communication link to a host PC.

The FTDI is connected to the UART of the module and presents it as a virtual COM port. Further, the FTDI can be used to program the SPI flash memory. On modules with a SoC or FPGA from Xilinx, the FTDI can be configured as JTAG programmer. The reference designs contain guides and examples for the different functionalities of the FTDI. By default, the UART communication between the FTDI device and FPGA is active. The Xilinx JTAG mode can be activated using the Enclustra MCT [11] and is independent of the UART connection.

The FTDI device is also connected to the system controller. Details on functions of the system controller can be found in Section 6.11.

6.3.4 USB Type-C

The USB Type-C connector on the Mercury+ PE3 base board supports host and device mode for USB 3.0, Power Delivery and DisplayPort alternate mode. To use the USB Type-C connector the MGT and USB multiplexer descibed in the previous sections need to be configured. In addition, the USB Type-C connector has a USB Type-C multiplexer which is controlled by the USB Type-C controller chip. If the Mercury+ PE3 base board is connected with another device via USB Type-C, the controller will negotiate with the other device, which functions are supported and configure the USB Type-C multiplexer accordingly. In order to advertise the correct features to other devices, the USB Type-C controller needs to know which functions are implemented on the Mercury+ PE3 base board. The configuration of the USB Type-C controller is described in the PE3 USB Type-C Application Note [13].

6.4 Buttons

All buttons are active-low; their function is described in Table 30.

For details, refer to the Mercury+ PE3 Base Board User Schematics [4].

Button Name	Button	Signal Name	Function	Comments
PWR	S2201	PWR_BTN#	Power-on/-off	Refer to Section 5.3
POR	S2104	POR#_LOAD#_BTN	Power-on reset/ Configuration-clear	Refer to the Enclustra Module Pin Connection Guidelines [8]
SRST	S2105	SRST#_BTN	Soft-reset/ Configuration-delay	Refer to the Enclustra Module Pin Connection Guidelines [8]
BTN	S2103	BTN#	User function	Connected to A-70 pin

Table 30: Board Buttons

6.5 DIP Switches

There are 12 configuration switches on the Mercury+ PE3 base board, grouped into 3 groups: CFG A, CFG B and CFG C.

Tables 31, 33 and 34 describe their functions; the factory default is marked in bold.

Warning!

Please note that the DIP switches must be configured according to the connectivity requirements. The factory default configuration does not implicitly indicate a valid configuration. The DIP switches may require different settings depending on the equipped module.

For details on the board configuration, refer to the Mercury+ PE3 Base Board User Schematics [4].

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG A 1	BOOT_MODE0	OFF	BOOT_MODE0 is set to 1	Refer to the Mercury module user manual
		ON	**BOOT_MODE0 is set to 0**	
CFG A 2	BOOT_MODE1	**OFF**	**BOOT_MODE1 is set to 1**	Refer to the Mercury module user manual
		ON	BOOT_MODE1 is set to 0	
CFG A 3	SCMODE0#_VMON_SEL	OFF	On startup: ScMode0 register is set to 1	Refer to Table 32 and Section 6.9
			After startup: VMON_SEL is set to 1	
		ON	**On startup: ScMode0 is set to 0**	
			After startup: VMON_SEL is set to 0	
CFG A 4	PWR_ON#	OFF	Power control ON	Refer to Section 5.3
		ON	**Power control OFF**	

Table 31: S2102 - Configuration Switch A

Some of the configuration switches have different functions, on startup and after startup; these switches are connected to the system controller, which reads the switch positions on startup and defines the behavior of certain circuit elements accordingly.

When powering the system controller, the switch has the "On startup" effect; afterwards the switch can be toggled to obtain the required hardware configuration.

Note that the system controller is powered when either a USB cable is attached, or when the main power is applied.

Table 32 describes the meaning of the ScMode0 register and its influence on the Mercury+ PE3 base board functionality. Details on these registers can be found in Section 6.11.

ScMode0 Register	Effect
0	The system controller has Xilinx JTAG functionality
1	The system controller has Altera JTAG functionality (currently not supported)

Table 32: ScMode0 Register Usage

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG B 1	USB_MODE0	**OFF**	**USB_MODE0 is set to 1**	Refer to Section 6.3
		ON	USB_MODE0 is set to 0	
CFG B 2	USB_MODE1	**OFF**	**USB_MODE1 is set to 1**	Refer to Section 6.3
		ON	USB_MODE1 is set to 0	
CFG B 3	USB_SEL	**OFF**	**USB_SEL is set to 1**	Refer to Section 6.3
		ON	USB_SEL is set to 0	
CFG B 4	USBC_SINK_EN#	**OFF**	**USBC_SINK_EN# is set to 0. Mercury+ PE3 base board is powered by USB Type-C.**	Refer to Section 6.3.4
		ON	USBC_SINK_EN# is set to 1. Mercury+ PE3 base board is not powered by USB Type-C.	

Table 33: S2100 - Configuration Switch B

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG C 1	DIP#	-	User-defined function	Connected to pin A-72
CFG C 2	SCMODE#_PCIE_SEL	**OFF**	**PCIe 0-3 are connected to MGT 4-7. PCIe 4-7 are connected to MGT 8-11. (use case: PL PCIe for XU*)**	MGT connections can be changed after boot via I2C
		ON	PCIe 0-3 are connected to MGT 0-3. PCIe 4-7 are connected to MGT 4-7. (use case: PS PCIe for XU*, PL PCIe for XU5-G1/ZX*/KX*/AA1/SA*)	
CFG C 3	USBCC_GPIO14	-	User-defined function	Connected to USB Type-C ctrl. and to the system ctrl.
CFG C 4	USBCC_GPIO15	-	User-defined function	

Table 34: S2101 - Configuration Switch C

6.6 I2C Communication

There are several I2C devices on the Mercury+ PE3 base board connected to two I2C buses.

- I2C_MGMT: All I2C devices which are used to configure board features are on this bus. The I2C_MGMT bus can access devices on the I2C_USER bus.
- I2C_USER: All I2C devices which are application-dependent are on this bus, e.g., Anios, SFP+, FMC, HDMI etc.

The Mercury module and the FTDI device can be I2C masters on the I2C_MGMT bus. I2C_MGMT connections are described in Table 35 and I2C_USER connections in Table 36. The I2C_USER connection is available directly at the module connector (pins A-55/57) or cascaded via I2C_MGMT channel 1.

Figure 21 illustrates the I2C connections corresponding to the information provided in Tables 35 and 36. Please note that all I2C addresses are written in a 7-bit hexadecimal format.

The USB Type-C multiplexer can be controlled by the I2C multiplexer channel 2 or by the USB Type-C controller - which is illustrated by the dotted line in Figure 21.

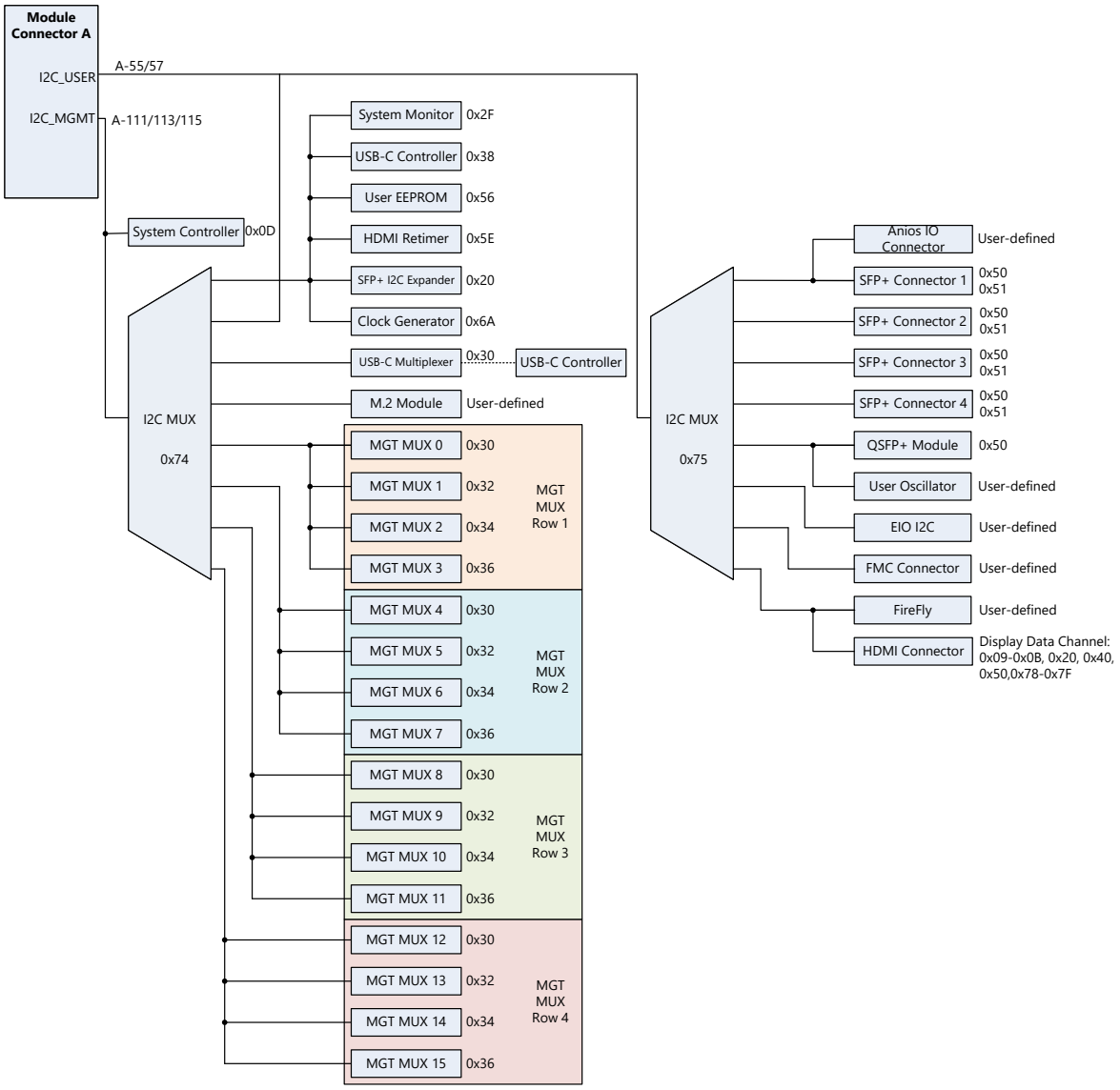


Figure 21: I2C Bus Structure and Devices

MGT MUX Row	I2C channel	Voltage	I2C Addr. (7-bit)	Device	Description	Des.
	MGMT	3V3_MOD		Module connector A		J200
	MGMT LS	3V3_AUX	0x0D	MachXO2	System controller	U400
	MGMT LS	3V3_AUX	0x74	PCA9547BSB	I2C multiplexer MGMT	U1901
	MGMT CH0	3V3_AUX	0x2F	LM96080CIMT	System monitor	U2501
	MGMT CH0	3V3_AUX	0x38	TPS65987-DDHRSHR	USB Type-C controller	U804
	MGMT CH0	3V3_AUX	0x56	24AA128T-I/MNY	User EEPROM	U1903
	MGMT CH0 LS	3V3	0x5E	SN65DP159RSB	HDMI retimer	U1500
	MGMT CH0 LS	3V3	0x20	PCA6416AHF	SFP I2C I/O expander	U1700
	MGMT CH0 LS	3V3	0x6A	SI5332A-D-GM3	Clock generator	U1802
	MGMT CH2	3V3_USBCC	0x30	CBTL08GP053-EVAZ	USB Type-C multiplexer	U707
	MGMT CH3	1V8	UD[2]	User-defined	M.2 module	J1400
MUX1	MGMT CH4	3V3	0x30	CBTL08GP053-EVAZ	MGT multiplexer 0	U1000
MUX1	MGMT CH4	3V3	0x32	CBTL08GP053-EVAZ	MGT multiplexer 1	U1001
MUX1	MGMT CH4	3V3	0x34	CBTL08GP053-EVAZ	MGT multiplexer 2	U1002
MUX1	MGMT CH4	3V3	0x36	CBTL08GP053-EVAZ	MGT multiplexer 3	U1003
MUX2	MGMT CH5	3V3	0x30	CBTL08GP053-EVAZ	MGT multiplexer 4	U1004
MUX2	MGMT CH5	3V3	0x32	CBTL08GP053-EVAZ	MGT multiplexer 5	U1005
MUX2	MGMT CH5	3V3	0x34	CBTL08GP053-EVAZ	MGT multiplexer 6	U1006
MUX2	MGMT CH5	3V3	0x36	CBTL08GP053-EVAZ	MGT multiplexer 7	U1007
MUX3	MGMT CH6	3V3	0x30	CBTL08GP053-EVAZ	MGT multiplexer 8	U1100
MUX3	MGMT CH6	3V3	0x32	CBTL08GP053-EVAZ	MGT multiplexer 9	U1101
MUX3	MGMT CH6	3V3	0x34	CBTL08GP053-EVAZ	MGT multiplexer 10	U1102
MUX3	MGMT CH6	3V3	0x36	CBTL08GP053-EVAZ	MGT multiplexer 11	U1103
MUX4	MGMT CH7	3V3	0x30	CBTL08GP053-EVAZ	MGT multiplexer 12	U1104

Continued on next page...

MUX4	MGMT CH7	3V3	0x32	CBTL08GP053-EVAZ	MGT multiplexer 13	U1105
MUX4	MGMT CH7	3V3	0x34	CBTL08GP053-EVAZ	MGT multiplexer 14	U1106
MUX4	MGMT CH7	3V3	0x36	CBTL08GP053-EVAZ	MGT multiplexer 15	U1107

Table 35: I2C_MGMT Structure

I2C channel	Voltage	I2C Address (7-bit)	Device	Description	Designator
USER	VCC_IO_A		Module connector A		
USER LS & MGMT CH1	3V3	0x75	PCA9547BSB	I2C multiplexer	U1900
USER CH0	3V3	UD[2]	User-defined	Anios IO connector	J2000
USER CH0	3V3	0x50/0x51	User-defined	SFP+ module 1	J1701
USER CH1	3V3	0x50/0x51	User-defined	SFP+ module 2	J1702
USER CH2	3V3	0x50/0x51	User-defined	SFP+ module 3	J1703
USER CH3	3V3	0x50/0x51	User-defined	SFP+ module 4	J1704
USER CH4	3V3	0x50	User-defined	QSFP+ module	J1700
USER CH4	3V3	UD[2]	User-defined	User oscillator	Y1801
USER CH5	3V3_MOD	UD[2]	User-defined	EIO I2C	J1200
USER CH6	3V3_MOD	UD[2]	User-defined	FMC connector	J1600
USER CH7	3V3	UD[2]	User-defined	FireFly module	J1402
USER CH7	5V0_HDMI	UD[2]	HDMI connector	HDMI DDC channel	U1500/J1501

Table 36: I2C_USER Structure

6.7 LEDs

The Mercury+ PE3 base board has a number of LEDs which either display a status or are user controlable. Figure 22 shows the position of the LEDs on the board and table 37 lists the purpose of each LED.

[2]UD = User-defined

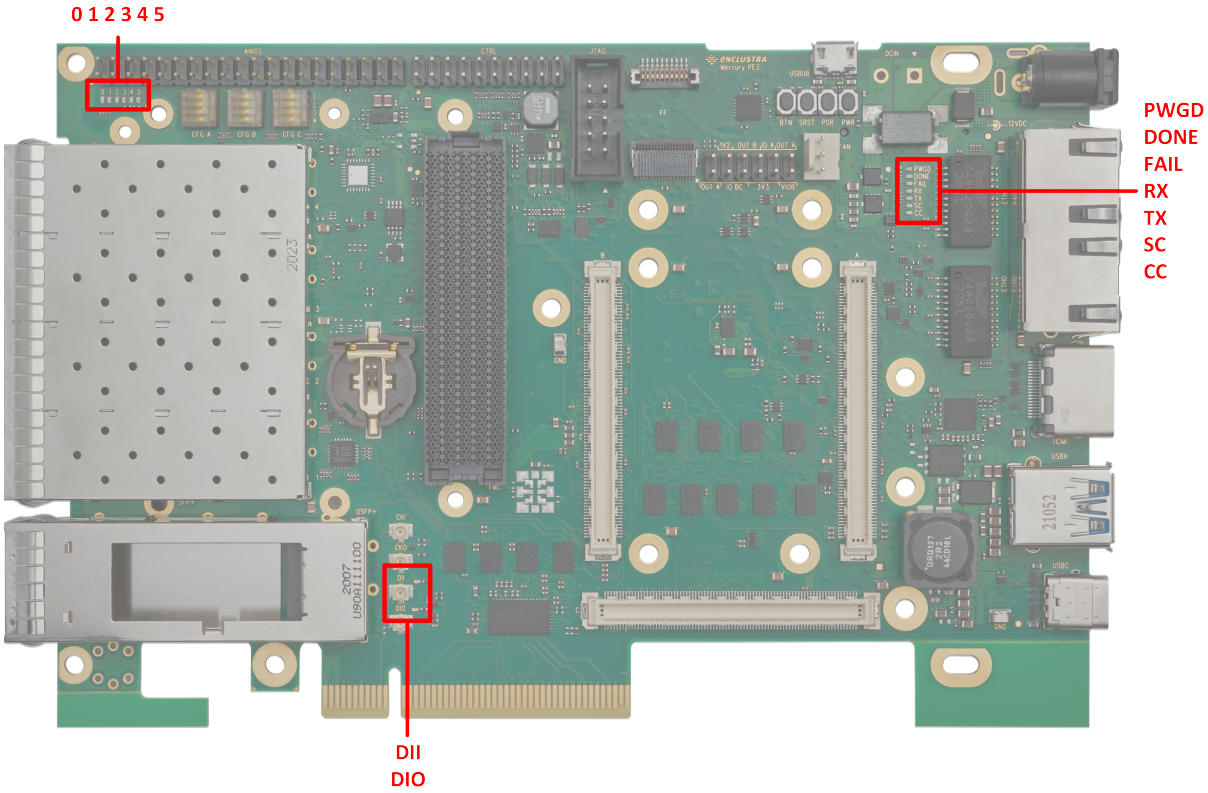


Figure 22: LED Position

LED Name	LED	Signal Name	Controlled by	Description
PWGD	D2100	PWR_OK#	Power circuits	Indicates that PWR_GOOD_IO is active and VCC_IO_A VCC_IO_BC are available
DONE	D2101	FPGA_DONE	Mercury module	FPGA configuration is done
FAIL	D2103	-	Power circuits	Indicates that one of the power supplies is failing, or the voltage configuration is incorrect
RX	D2110	RXLED#	System controller	UART RX status
TX	D2111	TXLED#	System controller	UART TX status
SC	D2112	SCLED#	System controller	System controller status
DII	D2108	DIILED#	Mercury module	User LED (shared with digital I/O input signal)
DIO	D2109	DIOLED#	Mercury module	User LED (shared with digital I/O output signal)
0	D2104	LED0#	Mercury module, System controller	User LED
1	D2105	LED1#	Mercury module, System controller	User LED
2	D2106	LED2#	Mercury module, System controller	User LED
3	D2107	LED3#	Mercury module, System controller	User LED
4	D2113	SC_LED4#	System controller	User LED
5	D2114	SC_LED5#	System controller	User LED
CC	D2115	USBCC_LED#	USB Type-C controller	User LED

Table 37: Board LEDs

For details on the LED connections, refer to the Mercury+ PE3 Base Board User Schematics [4].

6.8 SFP+ I2C Expander

A 16-bit I2C I/O expander device is used for controlling the SFP+ and QSFP+ status and configuration signals. This device is connected to the I2C bus, as described in Section 6.6. The interrupt pin of the I/O expander is connected to the I2C global interrupt line.

6.8.1 SFP+ I2C Expander Type

Table 38 describes the equipped SFP+ I2C I/O expander device type on the Mercury+ PE3 base board.

Type	Manufacturer
PCAL6416AHF,128	NXP

Table 38: SFP+ I2C I/O Expander Type

6.8.2 SFP+ I2C Expander Connectivity

Table 39 describes the signals connected to the I2C I/O expander. For additional information on the functions of the SFP+ and QSFP+ control and status signals, refer to the SFP+ and to QSFP+ standards.

Pin Name	Signal	Description
P0_0	SFP1_TXFAULT	SFP1 transmitter fault indication
P0_1	SFP1_TXDISABLE	SFP1 transmit disable
P0_2	SFP1_LOS	SFP1 loss of signal
P0_3	SFP2_TXFAULT	SFP2 transmitter fault indication
P0_4	SFP2_TXDISABLE	SFP2 transmit disable
P0_5	SFP2_LOS	SFP2 loss of signal
P0_6	SFP_RATE0	Rate Select 0, optionally controls SFP module receiver.
P0_7	QSFP_LPMODE	QSFP+ low power mode
P1_0	SFP3_TXFAULT	SFP3 transmitter fault indication
P1_1	SFP3_TXDISABLE	SFP3 transmit disable
P1_2	SFP3_LOS	SFP3 loss of signal
P1_3	SFP4_TXFAULT	SFP4 transmitter fault indication
P1_4	SFP4_TXDISABLE	SFP4 transmit disable
P1_5	SFP4_LOS	SFP4 loss of signal
P1_6	SFP_RATE1	Rate Select 1, optionally controls SFP module transmitter
P1_7	QSFP_MODPRS#	QSFP module is present

Table 39: SFP+ I2C I/O Expander Connectivity

Note that no short circuit protection is implemented for the SFP_RATE1 signal, which is required for the old generation of SFP+ modules, as described by the SFP standard.

6.9 System Monitor/Current Sense

The Mercury+ PE3 base board features a system monitor and current sense circuit, addressable via I2C - these are used for voltage and current monitoring. Additional functionality, such fan control, is also available.

Type	Manufacturer
LM96080	Texas Instruments

Table 40: System Monitor Type

The system monitor performs two sets of voltage and current measurements. The user can select which set of inputs should be measured by toggling the value of the VMON_SEL signal. This can be set via DIP switches, or via the system controller registers. Please refer to Sections 6.5 and 6.11 for details.

Table 41 lists the voltage measurements performed by the system monitor.

Board Reference	Signal Name	System Monitor Register	VMON_SEL	Comments
-	VMON_MAIN	IN0	0	5 - 12 V
-	VMON_3V3	IN1	0	3.3 V ±5%
-	VMON_5V	IN2	0	5 V ±5%
-	VMON_USBC_VBUS	IN3	0	Depending on USB Type-C power mode and connected device
-	VMON_CS_MOD	IN4	0	VCC_3V3_MOD current
-	VMON_1V2	IN5	0	1.2 V ±5%
J300.8	VMON_C8	IN6	0	Module dependent
J200.102	VMON_A102	IN0	1	Module dependent
J201.8	VMON_B8	IN1	1	Module dependent
J201.167	VMON_B167	IN2	1	Module dependent
J201.168	VMON_B168	IN3	1	Module dependent
-	VMON_CS_USBC	IN4	1	USB Type-C current sensor
-	VMON_1V8	IN5	1	1.8 V ±5%
-	VREF_CS_USBC	IN6	1	USB Type-C current sensor

Table 41: System Monitor Voltage Connections

Table 42 describes the fan connection of the system monitor.

Board Reference	Signal Name	System Monitor Register	Description
J2202.3	SYSMON_TACHO	FAN1	Fan speed sense signal

Table 42: System Monitor I/O and Fan Connections

6.10 User EEPROM

The Mercury+ PE3 base board features a user EEPROM which may be accessed via I2C. It can be used to store user data (e.g. a serial number) and can be accessed by the FPGA module and by the system controller. See section 6.6 for I2C connection details.

Type	Manufacturer
24AA128T-I/MNY	Microchip

Table 43: User EEPROM Type

6.11 System Controller

The Mercury+ PE3 base board is equipped with a Lattice CPLD, LCMXO2-4000HC, with the role of a system controller managing the default function of the board and providing additional functions required to operate various interfaces.

The PE3 System Controller User Manual [14] describes the different functions of the System Controller and how to configure them. Also the update procedure is descibed in the manual. The manual and the firmware for the system controller can be downloaded from the Enclustra download page.

7 Operating Conditions

7.1 Absolute Maximum Ratings

Table 44 indicates the absolute maximum ratings for Mercury+ PE3 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	-0.3 to 16	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mercury module user manual	
$T_{ambient}$	Ambient temperature range *	-10 to +75	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 44: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Table 45 indicates the recommended operating conditions for Mercury+ PE3 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	12	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mercury module user manual	
$T_{ambient}$	Ambient temperature range*	-10 to +75	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 45: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

8 Ordering and Support

8.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

8.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

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References

[1] Enclustra General Business Conditions
http://www.enclustra.com/en/products/gbc/
[2] Enclustra FPGA Manager IP Solution
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[3] Mercury+ PE3 Base Board IO Net Length Excel Sheet
→ Ask Enclustra for details
[4] Mercury+ PE3 Base Board User Schematics
→ Ask Enclustra for details
[5] Mercury+ PE3 Base Board Known Issues and Changes
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[13] Mercury+ PE3 USB Type-C App Note
→ Ask Enclustra for details
[14] Mercury+ PE3 System Controller User Manual
→ Ask Enclustra for details