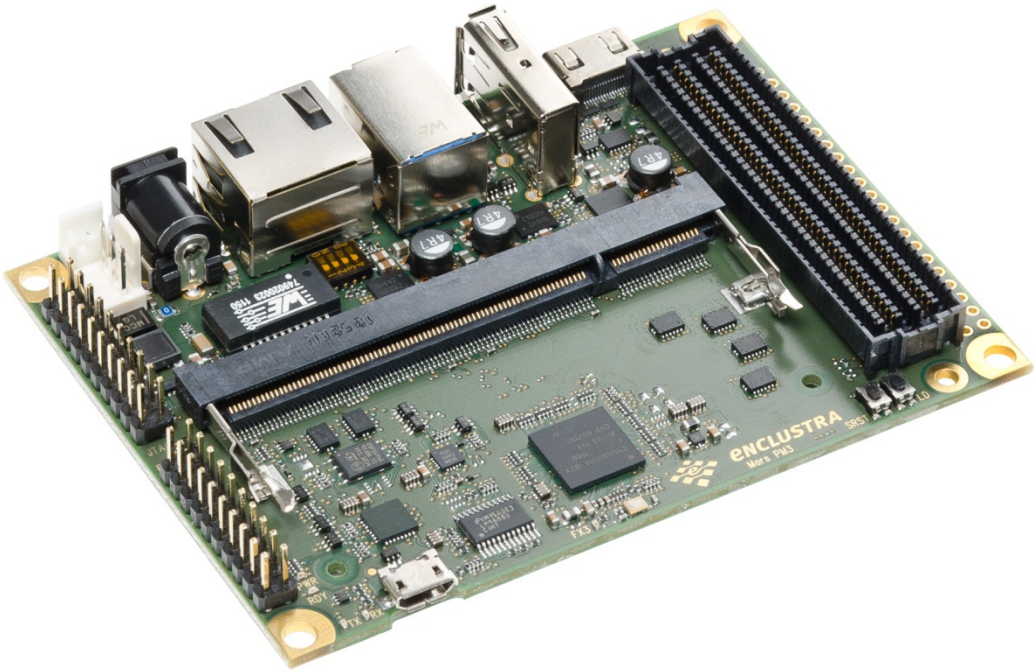
Mars PM3 (R1-R4)

User Manual



Project Info	
Project Manager	Martin Heimlicher
Author(s)	Silvio Ziegler
Reviewer(s)	Christoph Glattfelder
Version	1.08
Date	05.11.2018

Enclustra GmbH – Räffelstrasse 28 – CH- 8045 Zürich – Switzerland
Phone +41 43 343 39 43 – www.enclustra.com

Copyright reminder

Document History

Version	Date	Author	Comment
1.00	30.04.2012	S. Ziegler	First release
1.01	01.06.2012	S. Ziegler	Updated ambient temperature specification
1.02	25.06.2012	S. Ziegler	Updated technical data section
1.03	04.07.2012	S. Ziegler	Updated errata for R2
1.04	09.07.2012	S. Ziegler	Added more detailed info about FX3 boot mode options
1.05	03.08.2012	S. Ziegler	Added more details about Oscillator and boot mode configuration options
1.06	26.05.2014	C. Glattfelder	Added SD-Card
1.07	01.12.2016	C. Glattfelder	Added comment about R5 boards
1.08	05.11.2018	D. Ungureanu	Corrected I2C expander signals description

Table of Contents

1 Overview

This user manual only applies for Revision 4 boards and older. These boards have one DIP switch. If your Mars PM3 has two DIP switches please get the user manual for the R5 boards from our download page[1].

1.1 General

The Mars PM3 Board is equipped with a multitude of I/O interfaces for the use with the Mars FPGA and embedded processing module family. The board is equally well suited for rapid prototyping as well as for building low-quantity FPGA systems without the need of developing custom hardware.

Furthermore, the board can be used for production flashing of Mars modules or for educational purposes.

Benefits:

- Support for USB 3.0 device and USB 2.0 host
- High-Speed FPGA and flash programming over USB
- USB 3.0 to FPGA communication available in SPI, I^2C and 16 or 32 Bit slave FIFO modes
- 5 differential pairs per HDMI connector usable for various high-speed I/O applications
- I/O interfaces for almost all applications
- Industry-standard FMC low pin count connector
- Simple integration thanks to a single 12V supply voltage
- Alternatively, power can be supplied by the USB device port

1.1.1 Warranty

For information concerning the warranty please read through the "General Business Conditions" on Enclustra's website[2].

1.1.2 RoHS

The Mars module are designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.3 Disposal and WEEE

The Mars modules must be disposed properly at the end of its life span. If a battery is installed onto the board it must also be disposed correctly.

The Mars modules are not designed "ready for operation" for the end-user. The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars boards. Nonetheless users should still dispose the product properly at the end of life.

1.1.4 Safety Recommendations and Warnings

Ensure that the power supply is disconnected from the board before inserting or removing a Mars module, connecting interfaces, replacing SD-Cards and batteries, connecting jumpers, etc.

Take special care with the mounting orientation of Mars modules – they can fit in the connectors both ways round. The base board and the module may be damaged if inserted the wrong way and powered up.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage.

Over-voltage on power or signal lines can cause permanent damage.

1.1.5 Electro-Static Discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in an ESD protected environment.

1.1.6 EMC

This is a Class A product and is not intended to be used in domestic environments. The product may cause electromagnetic interference in which appropriate measures must be taken.

1.2 Deliverables

- Mars PM3 Board
- Mars PM3 user manual (this document)
- Mars PM3 schematics1

1.3 Accessories (Starter Kit Only)

- Mars MX1, MX2, AX3, ZX2 or ZX3 module respectively
- 12V Power Supply
- USB 3.0 A to B cable
- JTAG Adapter board for FX3 and FPGA debugging (JTAG-PM3)

2 Module Description

2.1 Block Diagram

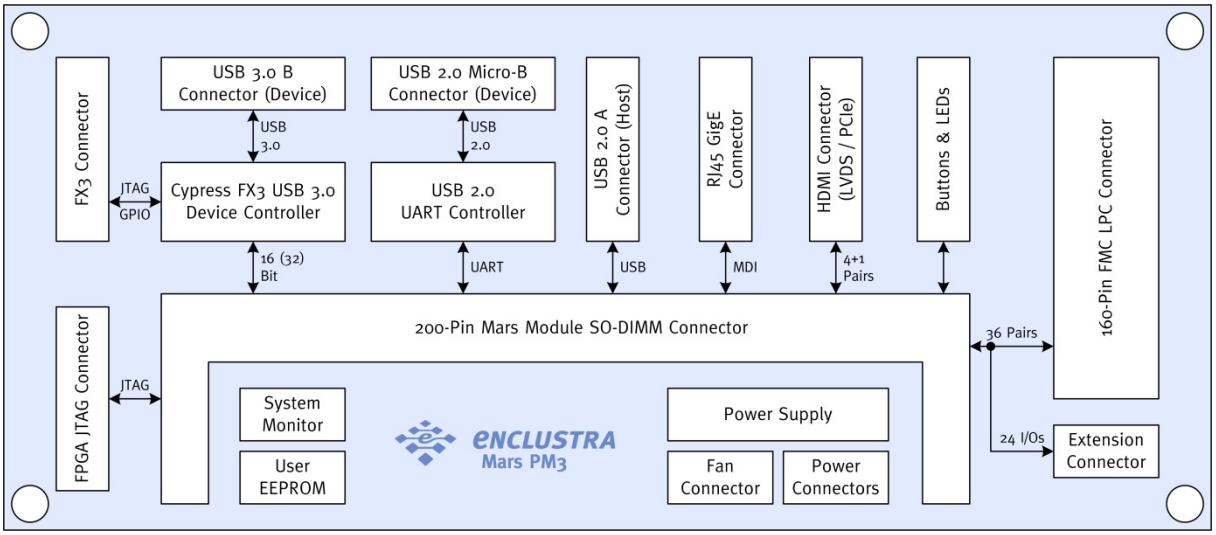


Figure 1: Mars PM3 board overview

2.2 Features

- Mars 200-pin SO-DIMM connector
- FMC low pin count connector
- Gigabit Ethernet RJ45 connector
- HDMI connector for PCIe or LVDS applications
- USB 3.0 B connector (device)
- USB 2.0 A (host) and Micro-B (device) connectors
- Cypress FX3 USB 3.0 device controller
- USB 2.0 High-Speed UART controller
- General purpose I/O connectors, fan connector, 2 push buttons, 5 LEDs
- Battery holder for real time clock
- SD-Card holder, connected to user IOs on FPGAs and bootable MIO pins on the Mars ZX3

Warning

Do not insert other SO-DIMM modules except Mars Enclustra FPGA Modules!

FMC restrictions apply when using 32 Bit FX3 interface

2.3 Part Numbers and Ordering Codes

Every module has a label with a marking specifying the part number and the serial number, as shown in Figure 2:

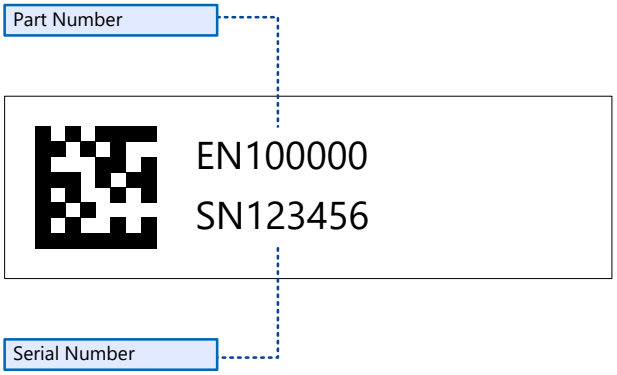


Figure 2: Module label

Table 1 shows the correspondence between part number and ordering code.

Part number	Ordering code
EN100581	MA-PM3-I-R3
EN100582	MA-PM3-C-R3
EN100745	MA-PM3-W-R4
EN100746	MA-PM3-C-R4
EN101233	MA-PM3-C-R5
EN101234	MA-PM3-W-R5

Table 1: Part Numbers and Ordering Codes

2.4 Top View

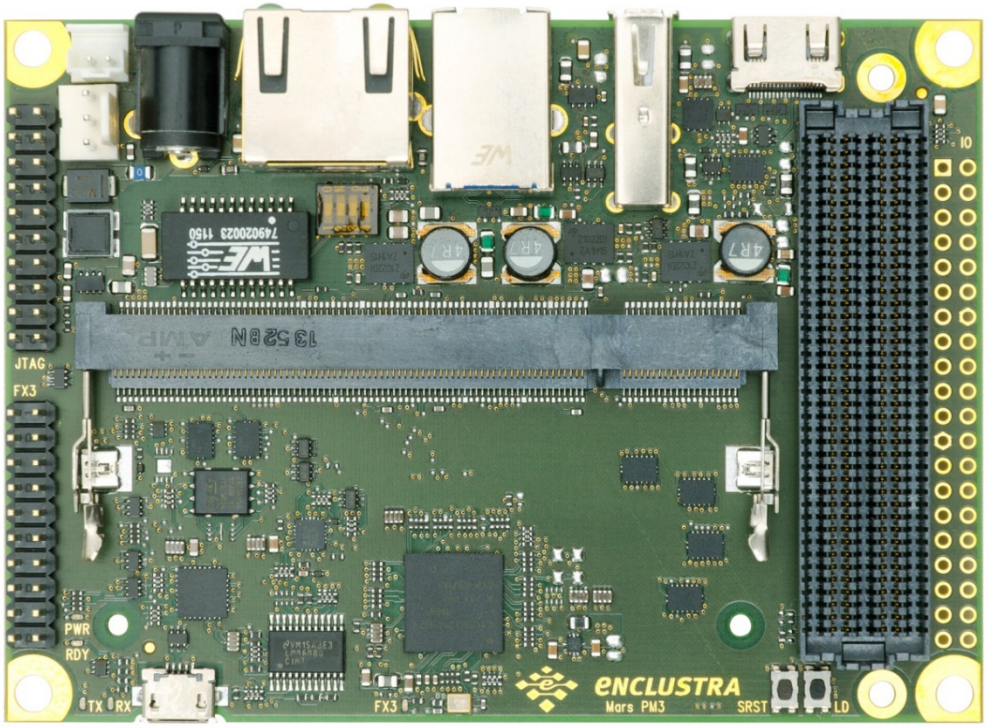


Figure 3: Top view

2.5 Bottom View

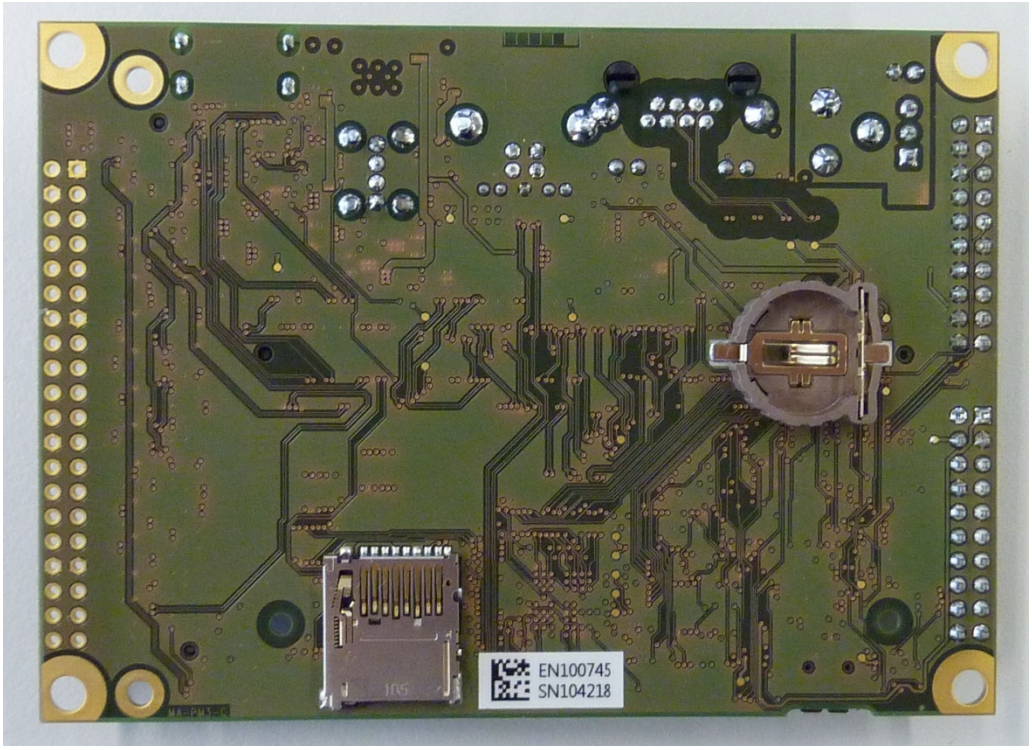


Figure 4: Bottom view

2.6 Dimensions

J800 (FPGA JTAG), J801 (FX3 Connector) and J1101 (IO Connector) are 2.54 mm pin headers.

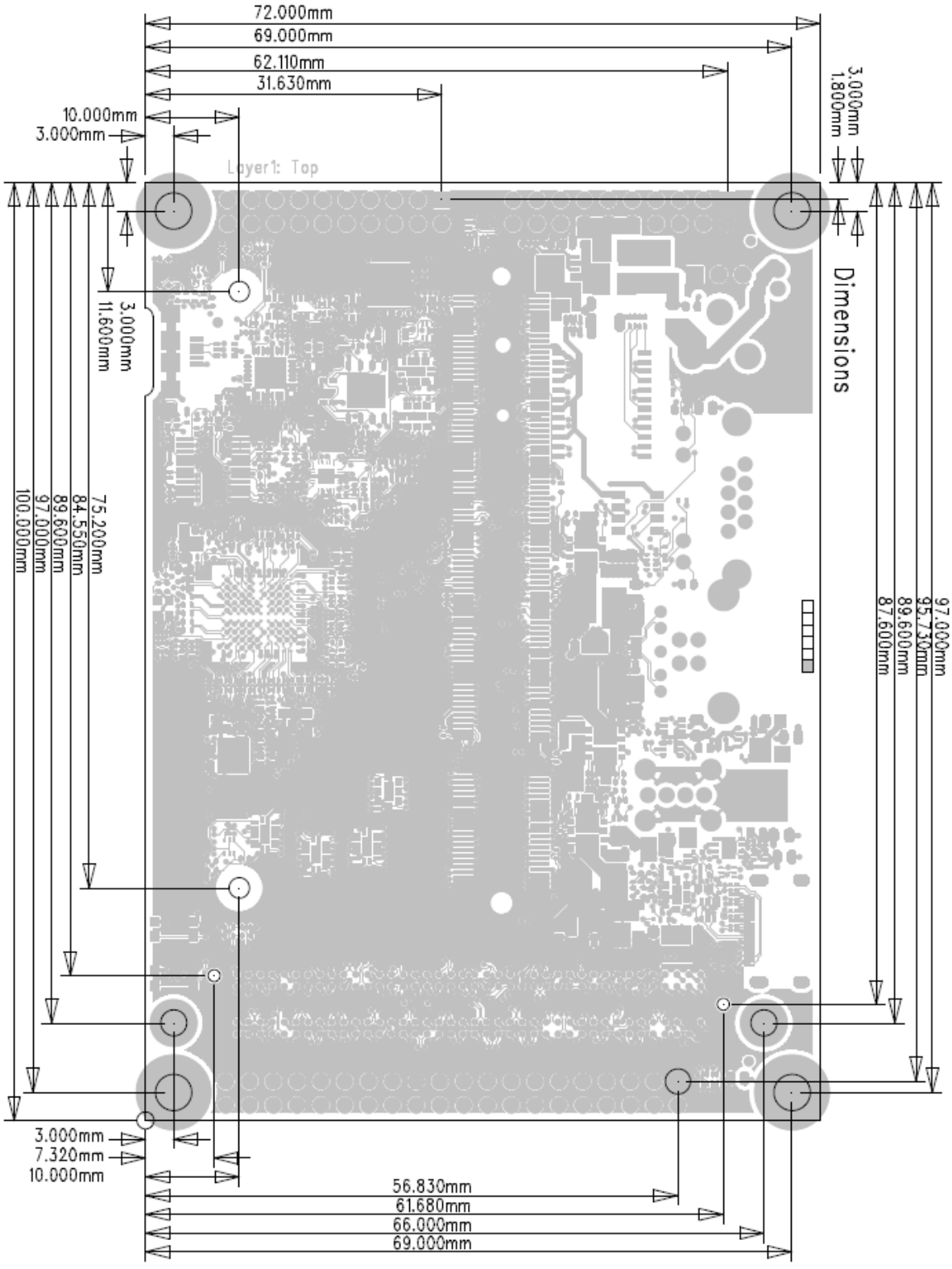


Figure 5: Dimensions

2.7 Assembly Drawing

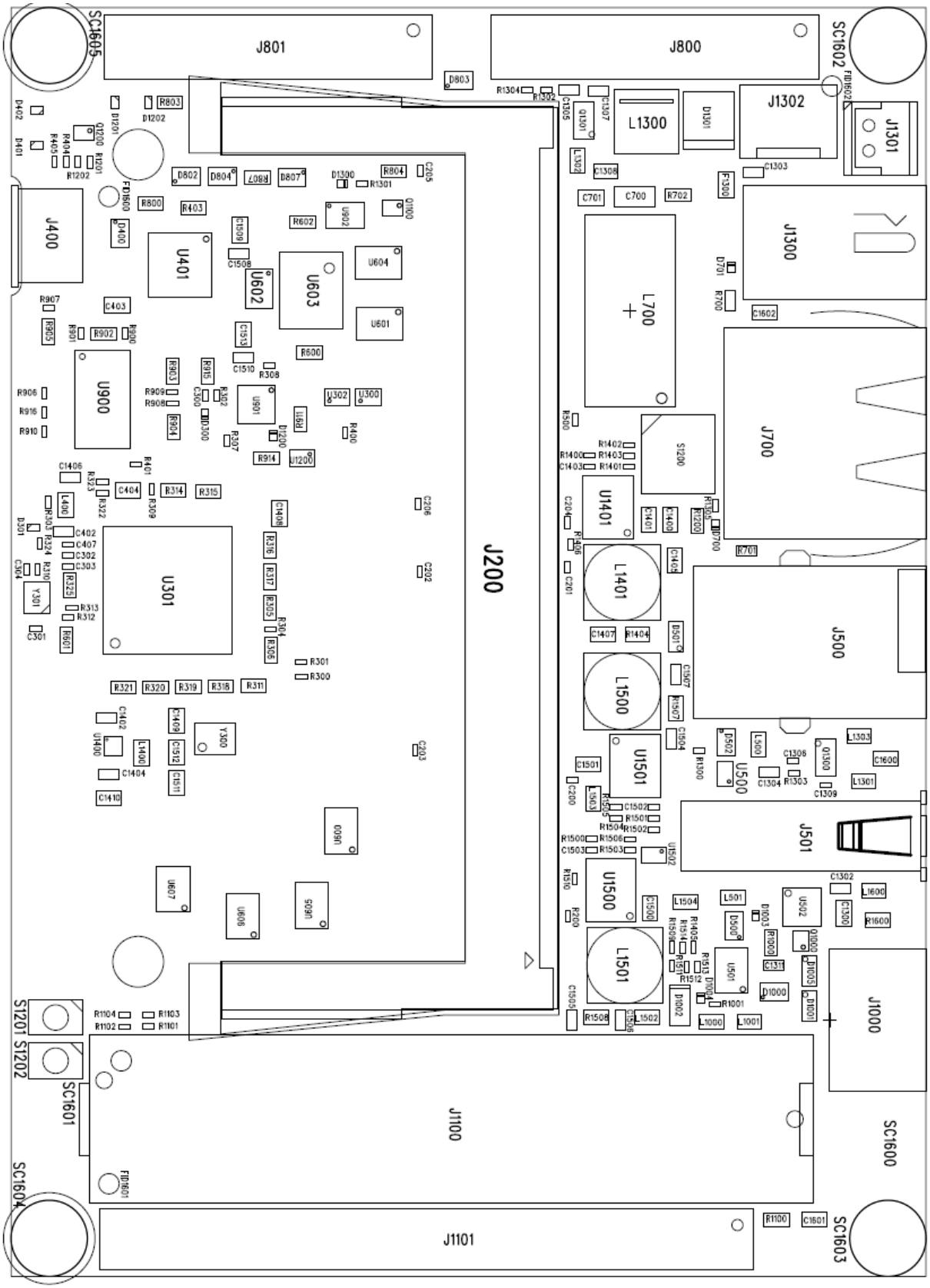


Figure 6: Assembly drawing top

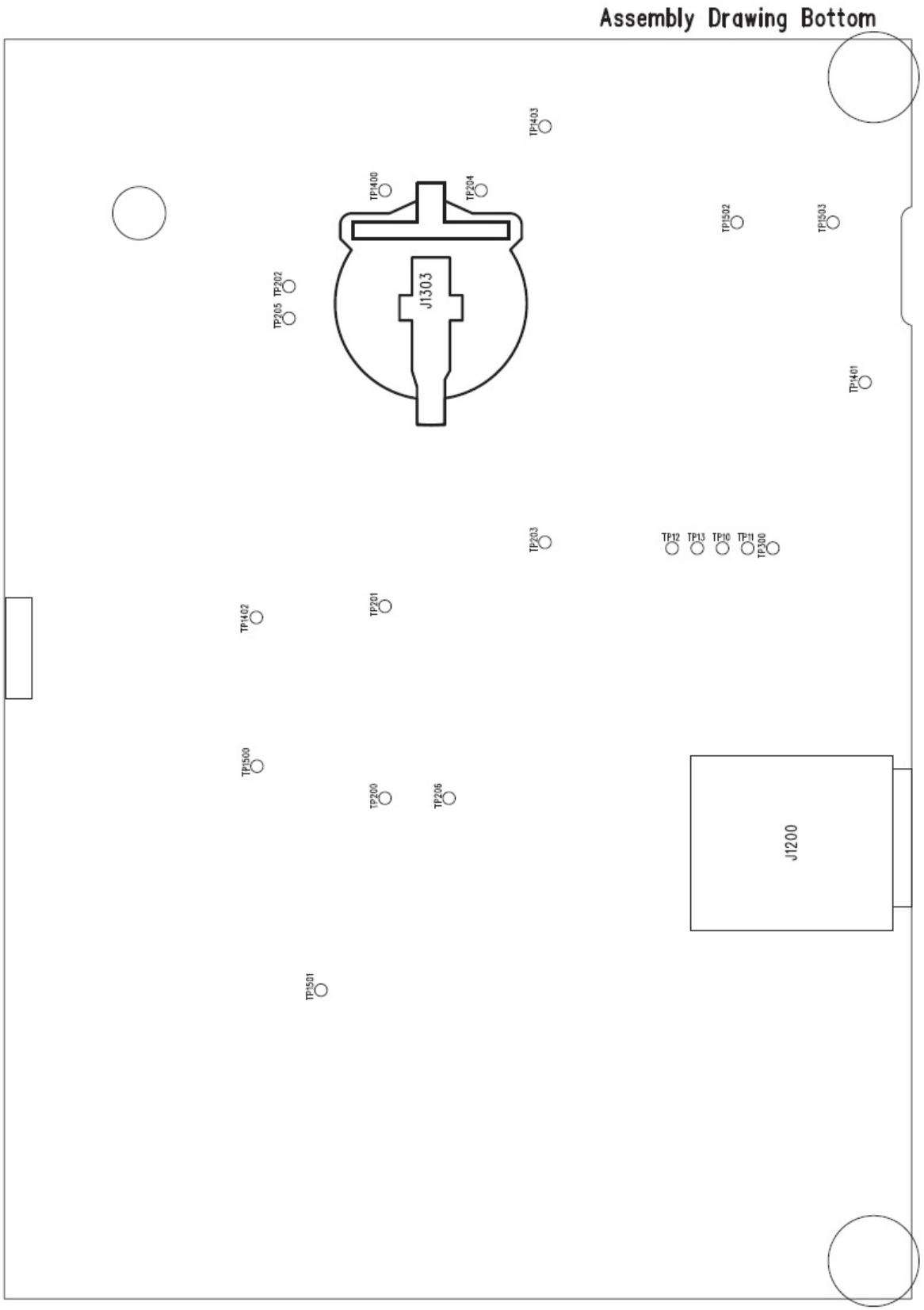


Figure 7: Assembly drawing bottom

2.8 DIP Switches

Table 2 shows the functions of the configuration DIP switch S1200. The options printed bold are the default settings.

Switch (S1200)	Off	On
1	**Mars MX2 Ethernet PHY or** **Mars ZX3 Ethernet PHY or** **Mars AX3 Ethernet PHY**	Mars MX1 Ethernet PHY
2	**VCC_IO is 2.5V**	VCC_IO is 3.3V
3	**USB from FPGA module routed to USB 2.0 A connector (J501)**	USB from FPGA module routed to USB 3.0 B connector J500 (FX3 USB connection disabled)
4	**Board powered from DC Power Input (J1300)**	Board powered from USB (J500) if J1300 not connected

Table 2: DIP switch S1200 settings

Warning
If DIP Switch S1200-4 is on (board powered from USB) then the board must not be powered from J1301 at the same time. Otherwise the Mars PM3 gets severely damaged.

2.9 Connector Pinouts

Table 3 shows an overview of all connectors assembled on the Mars PM3 Board. A more detailed description of each connector can be found further below in this section.

Connector	Description	Connected to
J200	Mars Module Connector	Mars FPGA module
J400	USB 2.0 Micro-B Connector	USB 2.0 UART Device (U401)
J500	USB 3.0 B Connector	Cypress FX3 USB 3.0 controller (U301) and Mars Module Connector
J501	USB 2.0 A Connector	Mars Module Connector
J700	RJ45 Ethernet Port (1G or 2x 100M)	Mars Module Connector
J800	FPGA JTAG Connector	Mars Module Connector

J801	FX3 Connector	Cypress FX3 USB 3.0 Controller (U301) and System Monitor
J1000	HDMI / PCIe Port	Mars Module Connector
J1100	FMC LPC Connector	Mars Module Connector
J1101	Extension Connector (not assembled)	Mars Module Connector
J1300	External Power Jack (12V DC, 2.1x5.5mm)	Power Supplies
J1301	Internal Power Connector	Power supplies
J1302	Fan Connector	System Monitor
J1303	Battery Holder	Mars Module Connector (RTC)

Table 3: Connector overview

2.9.1 J200 – Mars Module Connector

2nd Function	Signal	Connector Pin		Signal	2nd Function
	VCC_5V	1	2	GND	
	VCC_5V	3	4	FMC_CLK1_M2C_P	
	VCC_5V	5	6	FMC_CLK1_M2C_N	
	VCC_5V	7	8	GND	
	VCC_5V	9	10	PCIE_REFCLK_P	
	VCC_5V	11	12	PCIE_REFCLK_N	
	PGOOD_CARRIER	13	14	GND	
	GND	15	16	PCIE_PET1_P	
	PCIE_PER1_P	17	18	PCIE_PET1_N	
	PCIE_PER1_N	19	20	GND	
	GND	21	22	PCIE_PET0_P	
	PCIE_PER0_P	23	24	PCIE_PET0_N	
	PCIE_PER0_N	25	26	GND	
	GND	27	28	FMC_LA31_P	
	FMC_LA33_P	29	30	FMC_LA31_N	
	FMC_LA33_N	31	32	GND	
	GND	33	34	UART_TXD	
	FMC_LA32_P	35	36	UART_RXD	
	FMC_LA32_N	37	38	GND	

	GND	39	40	PGOOD_MODULE	
	MOD_VS3	41	42	MOD_VS1	
	FMC_LA17_CC_P	43	44	FMC_LA19_P	
	FMC_LA17_CC_N	45	46	FMC_LA19_N	
	GND	47	48	FMC_LA20_P	
	FMC_LA18_CC_P	49	50	FMC_LA20_N	
	FMC_LA18_CC_N	51	52	GND	
	VCC_IO	53	54	FMC_LA22_P	
	FMC_LA21_P	55	56	FMC_LA22_N	
	FMC_LA21_N	57	58	FMC_LA24_P	
	FMC_LA23_P	59	60	FMC_LA24_N	
	FMC_LA23_N	61	62	VCC_IO	
	GND	63	64	FMC_LA26_P	
	FMC_LA25_P	65	66	FMC_LA26_N	
	FMC_LA25_N	67	68	FMC_LA28_P	
	FMC_LA27_P	69	70	FMC_LA28_N	
	FMC_LA27_N	71	72	GND	
	VCC_IO	73	74	FMC_LA29_P	
	FMC_LA15_P	75	76	FMC_LA29_N	
	FMC_LA15_N	77	78	FMC_LA30_P	
	FMC_LA16_P	79	80	FMC_LA30_N	
	FMC_LA16_N	81	82	VCC_IO	
	GND	83	84	FMC_LA02_P	
	FMC_LA00_CC_P	85	86	FMC_LA02_N	
	FMC_LA00_CC_N	87	88	GND	
	MOD_VS2	89	90	FMC_LA03_P	FX3_DQ28
	FMC_LA04_P	91	92	FMC_LA03_N	FX3_DQ29
	FMC_LA04_N	93	94	1uF to GND	
	GND	95	96	FMC_LA05_P	FX3_DQ25
FX3_DQ24	FMC_LA06_P	97	98	FMC_LA05_N	FX3_DQ26
FX3_DQ27	FMC_LA06_N	99	100	GND	
	1uF to GND	101	102	FMC_LA07_P	
FX3_DQ31	FMC_LA01_CC_P	103	104	FMC_LA07_N	
FX3_DQ30	FMC_LA01_CC_N	105	106	MOD_VS4	
	GND	107	108	FMC_LA09_P	FX3_DQ18

FX3_DQ21	FMC_LA08_P	109	110	FMC_LA09_N	FX3_DQ16
FX3_DQ22	FMC_LA08_N	111	112	FMC_CLK0_M2C_P	
FX3_DQ19	FMC_LA10_P	113	114	FMC_CLK0_M2C_N	
FX3_DQ23	FMC_LA10_N	115	116	GND	
	VCC_IO	117	118	FMC_LA12_P	FX3_DQ20
	FMC_LA11_P	119	120	FMC_LA12_N	FX3_DQ17
	FMC_LA11_N	121	122	FMC_LA14_P	
	FMC_LA13_P	123	124	FMC_LA14_N	
	FMC_LA13_N	125	126	VCC_IO	
	GND	127	128	FX3_DQ13	
	FX3_FLAGB	129	130	FX3_DQ12	
	FX3_A1	131	132	FX3_DQ11	
	FX3_CLK	133	134	FX3_DQ14	
	FX3_FLAGA	135	136	GND	
	VCC_IO	137	138	FX3_DQ15	
SD_CLK	FX3_SLRD#	139	140	FX3_DQ9	
SD_CMD	FX3_SLWR#	141	142	FX3_DQ10	
SD_D0	FX3_SLOE#	143	144	FX3_DQ8	
SD_D1	FX3_PKTEND#	145	146	VCC_IO	
	GND	147	148	FX3_DQ7	
SD_D2	FX3_DQ3	149	150	FX3_DQ4	
SD_D3	FX3_DQ1	151	152	FX3_DQ6	
	FX3_DQ0	153	154	FX3_DQ5	
	FX3_DQ2	155	156	GND	
	GND	157	158	JTAG_TCK	
	USB_DP	159	160	JTAG_TDI	
	USB_DM	161	162	JTAG_TMS	
	USB_VBUS	163	164	JTAG_TDO	
	USB_ID	165	166	USB_CPEN	
	GND	167	168	Not Connected	
	ETH_A_N	169	170	Not Connected	
	ETH_A_P	171	172	GND	
	ETH0_LED1#	173	174	I2C_INT#	
	ETH0_LED2#	175	176	I2C_SDA	
	ETH_B_N	177	178	I2C_SCL	

	ETH_B_P	179	180	GND	
	ETH_CTREF	181	182	FPGA_CCLK	
	ETH_C_N	183	184	FPGA_DIN	
	ETH_C_P	185	186	FLASH_DI	
	ETH1_LED1#	187	188	FLASH_CS#	
	ETH1_LED2#	189	190	FPGA_MODE	
	ETH_D_N	191	192	FPGA_INIT#	
	ETH_D_P	193	194	FPGA_DONE	
	GND	195	196	FPGA_PROG#	
	VCC_3V3	197	198	MOD_VS5	
	VCC_3V3	199	200	VBAT	

Table 4: J200 – Mars module connector

2.9.2 J400 – USB 2.0 Micro-B Connector

The USB 2.0 Micro-B Connector J400 allows simple RS232 communication between a host computer and the Mars PM3 board using the USB interface. The USB 2.0 UART device U401 can be accessed from the host computer using a virtual COM port driver to display debug messages or sending control commands to the Mars PM3 board. The UART device is connected to the Mars module and the FX3 controller; make sure that the RX line is only driven by one device!

Power and data signals on this connector are protected against ESD incidents.

2.9.3 J500 – USB 3.0 B Connector

This USB connector can be used in two modes:

a) S1200-3 is off: The Cypress FX3 USB 3.0 controller's USB signals are routed to J500 and allow 300 MB/s high speed communication between the host computer and Mars PM3 Board.

b) S1200-3 is on: If the inserted Mars module features a USB controller, the USB signals of this module are routed to J500 to allow device mode operation. In this mode only USB 1.1 and 2.0 are supported.

This connector has the power and data signals protected against ESD incidents.

2.9.4 J501 – USB 2.0 A Connector

If the inserted Mars module features a USB controller, the USB signals of this module are connected to J501 and allow USB host mode operation. The power output on J501 can be switched on and off using the signal USB_CPEN that controls a USB load switch U502. Power and data signals on this connector are ESD protected.

2.9.5 J700 – RJ45 Ethernet

This connector can be operated in two modes:

a) If the inserted Mars module supports gigabit Ethernet, then this port provides one gigabit Ethernet link.

b) If the inserted Mars module supports dual 100 MBit Ethernet, then this port provides two 100 MBit Ethernet links using an external adapter.

It should be noted that depending on the Ethernet PHY of the inserted Mars module, the DIP switch S1200-1 has to be set according to Table 2. This connector is protected against ESD incidents.

2.9.6 J800 – FPGA JTAG Connector

The FPGA JTAG connector allows accessing the JTAG port of the inserted FPGA module. The signals on this connector are protected against ESD incidents.

For easier connection of the Xilinx and Altera JTAG programmers there is a breakout board with the standard connectors available. This adapter is included in the hardware kits only. If you order a single Mars PM3 please ask for a JTAG-PM3 if you need the adapter board.

Warning

The JTAG pins are connected to the FPGA with only small series impedance. Only apply VCC_IO compliant voltages to the IO pins. Any other voltages may damage the FPGA as well as other devices on the Mars PM3 Board or the installed Mars FPGA module.

Comment	Signal	Connector Pin		Signal	Comment
	VCC_IO	1	2	VCC_IO	
	FPGA_INIT#	3	4	GND	
	FPGA_TDI	5	6	GND	
	FPGA_TMS	7	8	GND	
	FPGA_TCK	9	10	GND	
	GND	11	12	GND	
	FPGA_TDO	13	14	GND	
	Not Connected	15	16	GND	
	Not Connected	17	18	GND	
	Not Connected	19	20	GND	

Table 5: J800 – FPGA JTAG connector

2.9.7 J801 – FX3 Connector

The main purpose of this connector is to access the JTAG port of the Cypress FX3 USB 3.0 controller. In addition, this connector feeds out four GPIO pins of the FX3 that can be used if the slave FIFO interface is not operated in 32 Bit mode. The SYSMON and VBAT signals are also accessible on this connector as well as the FX3 reset signal that can be pulled down to reset the Cypress FX3 USB controller. All signals on this connector are ESD protected.

Warning

The IO pins are directly connected to the Cypress FX3 USB 3.0 controller or other peripherals. Only apply VCC_IO compliant voltages to the IO pins. Any other voltages may damage the FX3 as well as other devices on the Mars PM3 Board.

Comment	Signal	Connector Pin		Signal	Comment
	VCC_12V	1	2	FX3_RESET_EXT#	
	GND	3	4	VCC_5V	
	VCC_3V3	5	6	FX3_FPGA_MODE	
	VBAT_IN	7	8	GND	
	SYSMON_GPI	9	10	SYSMON_GPO#	
	FX3_TRST#	11	12	FX3_GPIO0	
	FX3_TMS	13	14	FX3_GPIO1	
	FX3_TDO	15	16	FX3_GPIO2	
	FX3_TDI	17	18	FX3_GPIO3	
	FX3_TCK	19	20	GND	

Table 6: J801 – FX3 connector

2.9.8 J1000 – mini HDMI Connector

The signals on J1000 are connected to Multi-Gigabit-Transceivers, if available on the FPGA module. When using FPGA modules that do not support Gigabit-Transceivers, these signals can be used for high speed differential IOs (e.g. LVDS). The signals are directly routed to the FPGA (no AC coupling) with additional ESD protection. Some signals have alternative functions as indicated in the comments row. VCC_5V_HDMI is provided on the connector as 5V 150mA supply voltage.

Warning

The IO pins are directly connected to the FPGA. Only apply VCC_IO compliant voltages to the IO pins. Any other voltages may damage the FPGA as well as other devices on the Mars PM3 Board or the installed Mars FPGA module.

Comment	Signal	Connector Pin		Signal	Comment
	GND	1	2	PCIE_PER1_P	
	PCIE_PER1_N	3	4	GND	
	PCIE_PET0_P	5	6	PCIE_PET0_N	
	GND	7	8	PCIE_PER0_P	
	PCIE_PER0_N	9	10	GND	
	PCIE_REFCLK_P	11	12	PCIE_REFCLK_N	
	GND	13	14	PCIE_WAKE#	22k pull-up
I2C_SCL, 10k pull-up	PCIE_PERST#	15	16	PCIE_PRSNT	I2C_SDA, 10k pull-up

	PCIE_PET1_N	17	18	VCC_HDMI	5V 150mA
	PCIE_PET1_P	19	-	-	

Table 7: J1000 – mini HDMI connector

2.9.9 J1100 – FMC LPC Connector

This connector allows extending Mars PM3 boards with Enclustra (e.g. FMC DR2 Module) or third-party 160 pin LPC FMC modules.

Warning

The IO pins are directly connected to the FPGA. Only apply VCC_IO compliant voltages to the IO pins. Any other voltages may damage the FPGA as well as other devices on the Mars PM3 Board or the installed Mars FPGA module.

Comment	Signal	Connector Pin		Signal	Comment
	Not connected	H1	G1	GND	
	Not connected	H2	G2	FMC_CLK1_M2C_P	
	GND	H3	G3	FMC_CLK1_M2C_N	
	FMC_CLK0_M2C_P	H4	G4	GND	
	FMC_CLK0_M2C_N	H5	G5	GND	
	GND	H6	G6	FMC_LA00_CC_P	
	FMC_LA02_P	H7	G7	FMC_LA00_CC_N	
	FMC_LA02_N	H8	G8	GND	
	GND	H9	G9	FMC_LA03_P	FX3_DQ28
	FMC_LA04_P	H10	G10	FMC_LA03_N	FX3_DQ29
	FMC_LA04_N	H11	G11	GND	
	GND	H12	G12	FMC_LA08_P	FX3_DQ21
	FMC_LA07_P	H13	G13	FMC_LA08_N	FX3_DQ22
	FMC_LA07_N	H14	G14	GND	
	GND	H15	G15	FMC_LA12_P	FX3_DQ20
	FMC_LA11_P	H16	G16	FMC_LA12_N	FX3_DQ17
	FMC_LA11_N	H17	G17	GND	
	GND	H18	G18	FMC_LA16_P	
	FMC_LA15_P	H19	G19	FMC_LA16_N	
	FMC_LA15_N	H20	G20	GND	
	GND	H21	G21	FMC_LA20_P	
	FMC_LA19_P	H22	G22	FMC_LA20_N	

	FMC_LA19_N	H23	G23	GND	
	GND	H24	G24	FMC_LA22_P	
	FMC_LA21_P	H25	G25	FMC_LA22_N	
	FMC_LA21_N	H26	G26	GND	
	GND	H27	G27	FMC_LA25_P	
	FMC_LA24_P	H28	G28	FMC_LA25_N	
	FMC_LA24_N	H29	G29	GND	
	GND	H30	G30	FMC_LA29_P	
	FMC_LA28_P	H31	G31	FMC_LA29_N	
	FMC_LA28_N	H32	G32	GND	
	GND	H33	G33	FMC_LA31_P	
	FMC_LA30_P	H34	G34	FMC_LA31_N	
	FMC_LA30_N	H35	G35	GND	
	GND	H36	G36	FMC_LA33_P	
	FMC_LA32_P	H37	G37	FMC_LA33_N	
	FMC_LA32_N	H38	G38	GND	
	GND	H39	G39	VCC_IO	
	VCC_IO	H40	G40	GND	

Table 8: J1100A – FMC LPC connector

Comment	Signal	Connector Pin		Signal	Comment
	PGOOD_SYSTEM	D1	C1	GND	
	GND	D2	C2	Not Connected	
	GND	D3	C3	Not Connected	
	Not Connected	D4	C4	GND	
	Not Connected	D5	C5	GND	
	GND	D6	C6	Not Connected	
	GND	D7	C7	Not Connected	
FX3_DQ31	FMC_LA01_CC_P	D8	C8	GND	
FX3_DQ30	FMC_LA01_CC_N	D9	C9	GND	
	GND	D10	C10	FMC_LA06_P	FX3_DQ24
FX3_DQ25	FMC_LA05_P	D11	C11	FMC_LA06_N	FX3_DQ27
FX3_DQ26	FMC_LA05_N	D12	C12	GND	
	GND	D13	C13	GND	
FX3_DQ18	FMC_LA09_P	D14	C14	FMC_LA10_P	FX3_DQ19

FX3_DQ16	FMC_LA09_N	D15	C15	FMC_LA10_N	FX3_DQ23
	GND	D16	C16	GND	
	FMC_LA13_P	D17	C17	GND	
	FMC_LA13_N	D18	C18	FMC_LA14_P	
	GND	D19	C19	FMC_LA14_N	
	FMC_LA17_CC_P	D20	C20	GND	
	FMC_LA17_CC_N	D21	C21	GND	
	GND	D22	C22	FMC_LA18_CC_P	
	FMC_LA23_P	D23	C23	FMC_LA18_CC_N	
	FMC_LA23_N	D24	C24	GND	
	GND	D25	C25	GND	
	FMC_LA26_P	D26	C26	FMC_LA27_P	
	FMC_LA26_N	D27	C27	FMC_LA27_N	
	GND	D28	C28	GND	
	10k to VCC_3V3	D29	C29	GND	
	10k to VCC_3V3	D30	C30	FMC_I2C_SCL	
	Not Connected	D31	C31	FMC_I2C_SDA	
	VCC_3V3	D32	C32	GND	
	10k to VCC_3V3	D33	C33	GND	
	10k to GND	D34	C34	10k to GND	
	10k to VCC_3V3	D35	C35	VCC_12V	
	VCC_3V3	D36	C36	GND	
	GND	D37	C37	VCC_12V	
	VCC_3V3	D38	C38	GND	
	GND	D39	C39	VCC_3V3	
	VCC_3V3	D40	C40	GND	

Table 9: J1100B – FMC LPC connector

2.9.10 J1101 – Extension Connector (Not Assembled)

This connector can be assembled as an alternative to the LPC FMC Connector.

Warning

The IO pins are directly connected to the FPGA. Only apply VCC_IO compliant voltages to the IO pins. Any other voltages may damage the FPGA as well as other devices on the Mars PM3 Board or the installed Mars FPGA module.

Comment	Signal	Connector Pin		Signal	Comment
	GND	1	2	VCC_12V	
	VCC_3V3	3	4	GND	
	FMC_LA30_P	5	6	FMC_LA30_N	
	FMC_LA28_P	7	8	FMC_LA28_N	
	FMC_LA29_P	9	10	FMC_LA29_N	
	FMC_LA24_P	11	12	FMC_LA24_N	
	GND	13	14	VCC_IO	
	FMC_LA21_P	15	16	FMC_LA21_N	
	FMC_LA17_CC_P	17	18	FMC_LA17_CC_N	
	FMC_LA15_P	19	20	FMC_LA15_N	
	FMC_LA16_P	21	22	FMC_LA16_N	
	VCC_IO	23	24	GND	
	FMC_LA07_P	25	26	FMC_LA07_N	
	FMC_LA04_P	27	28	FMC_LA04_N	
	FMC_LA02_P	29	30	FMC_LA02_N	
	FMC_LA00_CC_P	31	32	FMC_LA00_CC_N	
	GND	33	34	GND	
	FMC_CLK0_M2C_P	35	36	FMC_CLK0_M2C_N	
	IO_I2C_EN	37	38	I2C_SDA	
	I2C_INT#	39	40	I2C_SCL	

Table 10: J1101 – Extension connector

2.9.11 J1200 – SD-Card

The SD-Card holder was added in release 3 of the Mars PM3 but not equipped by default. From revision 4 the SD-Card is equipped on all modules.

Since the SD-Card holder was added subsequently on bootable pins (MIO40..45) of the Mars ZX3, it shares the pins with the FX3 USB3 controller. Therefore SD-Card and USB3 can't be used simultaneously.

Connector Pin	Signal
Data 0	FX3_SLOE#
Data 1	FX3_PKTEND#
Data 2	FX3_DQ3
Data 3	FX3_DQ1
Clk	FX3_SLRD#
CMD	FX3_SLWR#
CD	Card detect is not connected

Table 11: J1200 – SD-Card

2.9.12 J1300 – Power Connector

Apply only 12V DC to this connector. The dimensions of the plug are 2.1x5.5mm

Connector Pin	Signal
Inner	VCC_12V_IN
Outer	GND
SW	USB_PWR_EN_SW# (Disables board supply from USB)

Table 12: J1300 – Power connector

2.9.13 J1301 – Internal Power Connector

This power connector can be used as an alternative to J1300. Apply only 12V DC to this connector. The connector type is TE-Connectivity 292132-2.

Warning
Never apply power to this connector if DIP switch S1200-4 is set to USB power mode (switch is on). Otherwise the Mars PM3 module will get severely damaged.

Connector Pin	Signal
1	VCC_12V_IN
2	GND

Table 13: J1301 – Internal power connector

2.9.14 J1302 – Fan Connector

At this connector a 12V fan with sense signal can be installed.

Connector Pin	Signal
1	GND
2	VCC_12V
3	SYSMON_TACHO (Sense signal to determine fan speed)

Table 14: J1302 – Fan connector

2.9.15 J1303 – Battery Holder

In this battery holder a 3V CR1220 battery for the FPGA module RTC can be installed. The battery holder was not equipped in boards prior revision R4.

Connector Pin	Signal
1	GND
2	VBAT_IN

Table 15: J1303 – Battery holder

2.10 Hardware description

This section gives an overview of the Mars PM3 Board features. More detailed information can be found in the Mars PM3 Board schematics[3].

2.10.1 Command Buttons

Button	Description
SRST (S1201)	Soft Reset: This active low button is connected to the FPGA through J200B, pin 192 (FPGA_INIT#) and may be used as a soft reset or any other function.
LD (S1202)	Load Firmware: This active low button is connected to the PROG_N/CONFIG_N pin of the FPGA. It forces the FPGA to clear the current configuration. A reconfiguration is required after pressing PROG#.

Table 16: Command buttons

2.10.2 Flash Configuration Multiplexer

The Cypress FX3 USB 3.0 controller has its own SPI flash, where it can load the application and / or VID and PID during startup. If no valid boot image is found, the FX3 is waiting to receive the application code over USB.

In addition, the FX3 can get control over the FPGA configuration interface, JTAG interface and SPI flash of the Mars FPGA modules by means of analogue multiplexers as shown in Figure 8. This allows configuring the FPGA over USB or programming the SPI flash from a PC without any additional hardware. The available multiplexer settings are shown in Table 17.

Warning

By default the flash configuration multiplexers should be kept in high impedance state to allow the FPGA to load the bitstream from the flash and debugging over JTAG using an external JTAG adapter cable connected to J800. Before changing the state of the multiplexers ensure that the accessed signals are not actively driven by another source. Before initializing the GPIOs of the FX3, the multiplexers are set to FX3 flash access to enable the Cypress FX3 USB 3.0 controller to boot from flash.

SPI_SEL	SPI_JTAG_EN#	SPI_CONFIG_EN#	Function
X	0	0	Not allowed
0	0	1	FPGA JTAG access
0	1	0	FPGA passive serial configuration
X	1	1	No access (high impedance)
1	0	1	FX3 Flash access
1	1	0	FPGA Flash access

Table 17: Flash configuration multiplexer settings

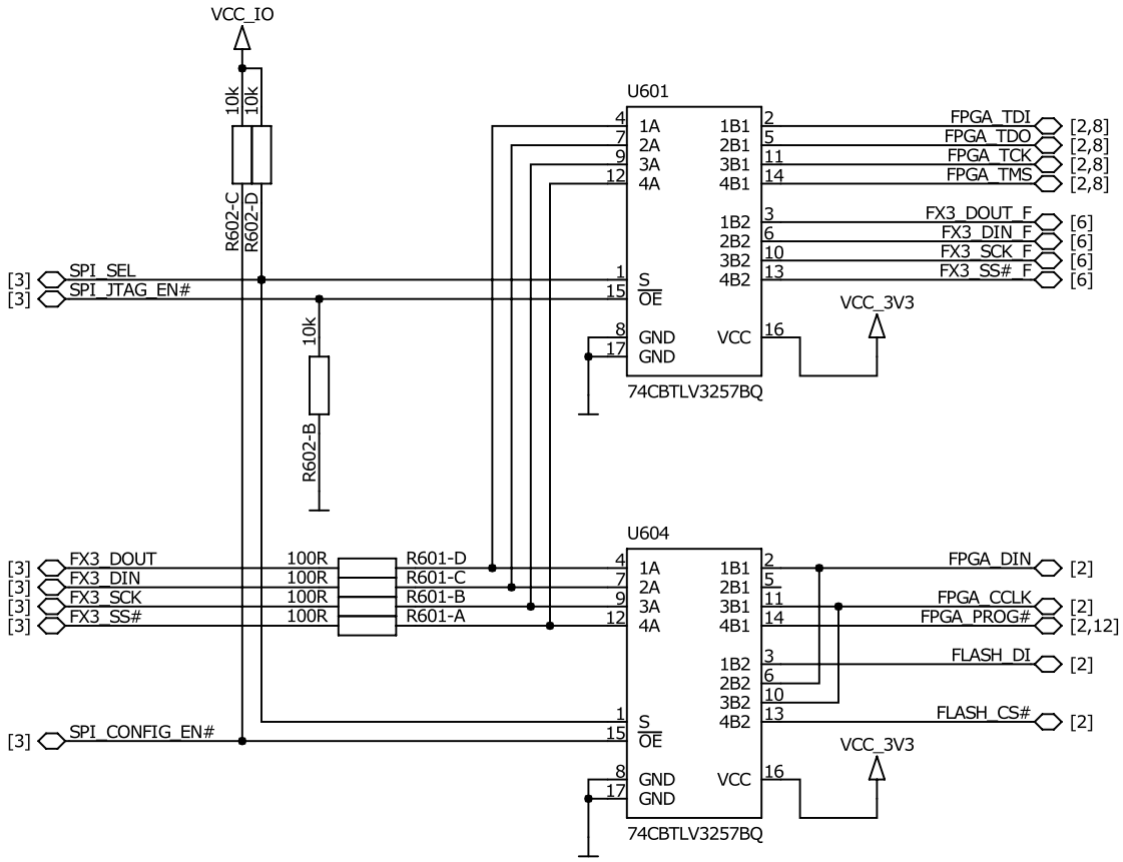


Figure 8: Flash configuration multiplexer

The control signals SPI_SEL, SPI_JTAG_EN# and SPI_CONFIG_EN# are connected to the Cypress FX3 USB 3.0 controller. For details refer to section 2.10.9.

2.10.3 Fifo Mode Multiplexer

The slave fifo interface between the FPGA module and the Cypress FX3 USB 3.0 controller can be operated either in 16 or 32 Bit mode. The FX3_PMODE0 signal allows selecting between those two modes. If 32 Bit mode is chosen, the usable differential signals on the FMC connector are reduced. In 16 Bit mode, the Cypress FX3 controller can access the USB 2.0 UART controller using its RS232 interface and four of its GPIO pins are routed to the FX3 connector (J801).

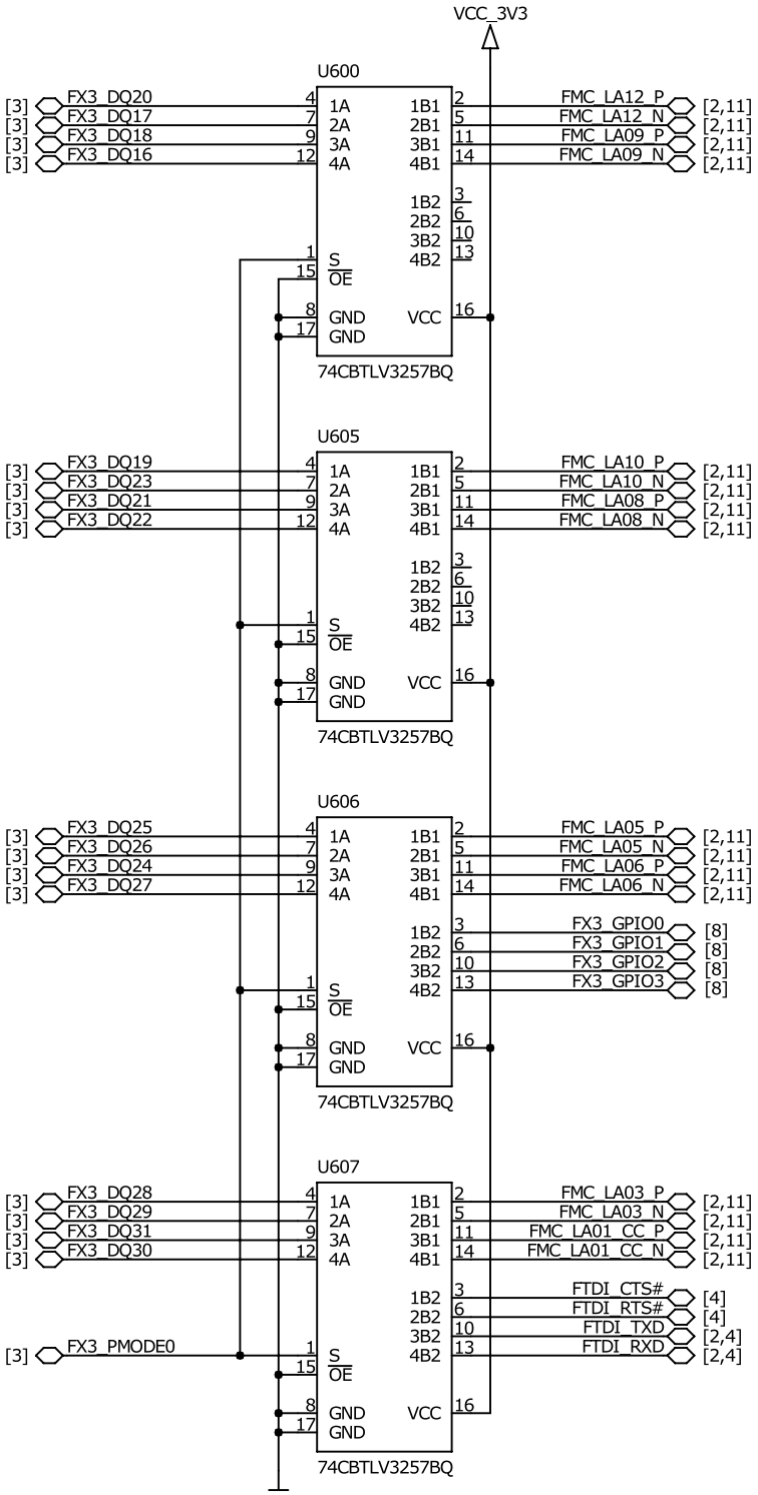


Figure 9: FIFO mode multiplexer

The control signal FX3_PMODE0 is connected to the Cypress FX3 USB 3.0 controller. For details refer to section 2.10.9.

2.10.4 LEDs

LED	Description
PWR (D1202)	Power Good: Indicates that DC-DC converters are in regulation.
RDY (D1201)	FPGA Ready: The RDY LED shows the configuration status of the FPGA. The LED is on when a valid bitstream is loaded and off if no bitstream has been loaded or the FPGA configuration has failed.
RX (D401)	Can be configured to indicate receive activity of the USB 2.0 UART USB Device.
TX (D402)	Can be configured to indicate transmit activity of the USB 2.0 UART USB Device.
FX3 (D301)	FX3 LED: Can be controlled by the user application running on the Cypress FX3 USB 3.0 controller.

Table 18: LEDs

2.10.5 I²C IO Expander

A Semtech SX1505 I²C IO Expander (U901) is used to read and control the following signals:

- Set the state of the slave fifo address signal A0 and chip select signal SLCS#
- Read the state of the PCIe reset signal PCIE_PERST#
- Read the state of the FX3_USB_SEL signal (chooses device or host connector for the USB signals coming from the FPGA module)
- Read the state of the USB_CPEN signal (enables power to the USB 2.0 host connector)
- Enable or disable the I²C bus on the HDMI or LPC FMC and extension connector respectively by means of PCIE_I2C_EN and IO_I2C_EN signals.
- Disable the write-protect signal of the user EEPROM

It uses the I²C address 0x21 (7 bit) and is connected to the I²C pins of the FPGA module and FX3.

For simple IO operations only the following two 8 bit registers are used. For more information about the SX1505 please refer to the SX150x[4] datasheet.

Register	Name	Description
0	Data	Read or write data
1	Direction	Direction (0=output, 1=input)

Table 19: I2C expander registers

Table 20 shows the connection of the I²C expander's GPIO pins.

I/O Bit	Signal	Description
I/O[0]	PCIE_PERST#	PCIe reset signal
I/O[1]	10k Pull up	EEPROM_WP signal (user EEPROM write-protect signal)
I/O[2]	FX3_SLCS#	Slave fifo chip select
I/O[3]	FX3_A0	Slave fifo address bit 0
I/O[4]	USB_CPEN	USB 2.0 power enable (Host connector J501)
I/O[5]	FX3_USB_SEL	1: USB signals from FPGA module routed to J500 (USB 3.0 disabled) 0: USB signals from FPGA module routed to J501 (USB 3.0 routed to J500)
I/O[6]	PCIE_I2C_EN	Enable signal for I²C bus on HDMI connector
I/O[7]	IO_I2C_EN	Enable signal for I²C bus on FMC and extension connector

Table 20: I²C expander I/O port assignment

2.10.6 RTC Battery

The battery on the Mars PM3 Board is used for the real time clock on the FPGA module. A 3V CR1220 battery can be placed here if needed. The battery holder was not assembled on older versions.

2.10.7 I²C EEPROM

A Microchip 128 kBit EEPROM (U902) is connected to the I²C bus on the Mars PM3 Board. It listens to address 0x54 (7 bit) and can be used to store user data (e.g. a serial number) and can be accessed by the FPGA and the Cypress FX3 USB 3.0 controller. For more details refer to the 24AA128 datasheet[5].

Type	Manufacturer
24AA128	Microchip

Table 21: I²C EEPROM Type

The write-protect signal of the user EEPROM is equipped with a 10k pull-up and it is connected to the I2C GPIO expander. By default, the EEPROM is write-protected. To allow write operations, this signal must be pulled low from the I2C expander.

2.10.8 System Monitor

An I²C system monitor (U1100) at address 0x2F is available on the Mars PM3 I²C bus to monitor the supply voltages (1V2, 3V3, VCC_IO, 5V and 12V), read the FAN RPM's and control two user GPIOs. It can be accessed by the FPGA and the Cypress FX3 USB 3.0 controller. For more details refer to the LM96080 datasheet[6].

Type	Manufacturer
LM96080	National

Table 22: I²C System Monitor Type

Pin	Signal	Direction	Description
21	IN0	IN	0.1754 * VCC_12V
20	IN1	IN	0.3125 * VCC_5V
19	IN2	IN	0.6875 * VCC_3V3
18	IN3	IN	0.6875 * VCC_IO
17	IN4	IN	1.0 * VCC_1V2
16	IN5	IN	1.0 * MOD_VS3
15	IN6	IN	1.0 * MOD_VS2
6	BTI		Not connected
7	GPI	IN	SYSMON_GPI
1	INT_IN#	IN	LOADSW_FLG# (0: USB 2.0 host and HDMI power failure, 1: Ok)
4	FAN1	IN	SYSMON_TACHO
5	FAN2	IN	Not connected
10	INT#	IN	I2C_INT#
11	GPO#	OUT	SYSMON_GPO#
12	RESET_IN#	IN	PGOOD_SYSTEM

Table 23: I²C System monitor pin assignment

2.10.9 Cypress FX3 USB 3.0 Controller

The Mars PM3 board features a USB 3.0 controller from Cypress, which allows data transfers to the host computer beyond 300 MB/s. The USB controller is connected to the FPGA module using a slave FIFO interface that can be configured for 16 or 32 Bit mode at an interface clock of 100 MHz. The USB

3.0 controller includes a 32 Bit ARM926 core operating at 200 MHz using a 19.2 MHz crystal oscillator. It can access the I^2C bus, SPI flash of the FPGA and exchange debug or control information with the USB 2.0 UART controller over UART. A JTAG interface is available on connector J801 to debug and download the application.

By default, the PMODE pins of the FX3 are configured for SPI boot with USB fall back (refer to Table 24). Hence, the application code can be stored in a dedicated 16 Mbit SPI flash that is read during startup. If no valid boot image is found, the FX3 tries to load the application from USB. By removing R301 and assembling 10 k to R300, the boot mode can be set to USB boot only.

PMODE[2:0]	Boot from	Comments
F00	Sync ADMUX (16 Bit)	Not selectable
F01	Async ADMUX (16 Bit)	Not selectable
F11	USB boot	Remove R301 and assemble 10 k to R300
F0F	Async RAM (16 Bit)	Not selectable
F1F	I^2C, on failure USB boot is enabled	Not selectable
1FF	I^2C only	Not selectable
0F1	**SPI, on failure USB boot is enabled**	**Default**

Table 24: Boot mode settings

For more details refer to the CYUSB3014 datasheet and documentation[7].

Type	Manufacturer
CYUSB3014	Cypress

Table 25: USB 3.0 Controller Type

Pin	Signal	Direction	Voltage	Description
J6	FX3_CLK	IN	VCC_IO	Slave fifo clock
K8	FX3_SLCS#	IN	VCC_IO	Slave fifo chip select
K7	FX3_SLWR#	IN	VCC_IO	Slave fifo write enable
J7	FX3_SLOE#	IN	VCC_IO	Slave fifo output enable
H7	FX3_SLRD#	IN	VCC_IO	Slave fifo read enable
G7	FX3_FLAGA	OUT	VCC_IO	Slave fifo Flag A

G6	FX3_FLAGB	OUT	VCC_IO	Slave fifo Flag B
K6	SPI_SEL	OUT	VCC_IO	Flash configuration multiplexer select
H8	FX3_PKTEND#	IN	VCC_IO	Slave fifo packet end
G5	SPI_JTAG_EN#	OUT	VCC_IO	Flash configuration multiplexer enable
H6	SPI_CONFIG_EN#	OUT	VCC_IO	Flash configuration multiplexer enable
K5	FX3_FPGA_MODE	OUT	VCC_IO	Set 0 to pull down FPGA_MODE signal
J5	FX3_A1	IN	VCC_IO	Slave fifo address signal 1
H5	FX3_A0	IN	VCC_IO	Slave fifo address signal 0
G4	FX3_PMODE0	IN / OUT	VCC_IO	DQ Multiplexer select
L8	INT#			Not connected
C5	FX3_RESET#	IN	VCC_3V3	Reset input
D9	I2C_SCL	IN / OUT	VCC_3V3	I^2C clock
D10	I2C_SDA	IN / OUT	VCC_3V3	I^2C data
D1	FPGA_DONE	IN	VCC_IO	FPGA done signal
D2	FPGA_INIT#	IN	VCC_IO	FPGA init signal
D3	I2C_INT#	IN / OUT	VCC_3V3	I^2C interrupt line
D4	FX3_SCK	OUT	VCC_3V3	SPI clock
C1	FX3_SS#	OUT	VCC_3V3	SPI select
C2	FX3_DIN	IN	VCC_3V3	SPI data in
D5	FX3_DOUT	OUT	VCC_3V3	SPI data out
C4	FX3_LED	OUT	VCC_3V3	User LED (1: on, 0: off)
C9	OTG			Not connected
D6	CLKIN_32	IN	VCC_3V3	Optional watchdog clock
F10	FX3_DQ0	IN / OUT	VCC_IO	Slave fifo data 0
F9	FX3_DQ1	IN / OUT	VCC_IO	Slave fifo data 1
F7	FX3_DQ2	IN / OUT	VCC_IO	Slave fifo data 2
G10	FX3_DQ3	IN / OUT	VCC_IO	Slave fifo data 3

G9	FX3_DQ4	IN / OUT	VCC_IO	Slave fifo data 4
F8	FX3_DQ5	IN / OUT	VCC_IO	Slave fifo data 5
H10	FX3_DQ6	IN / OUT	VCC_IO	Slave fifo data 6
H9	FX3_DQ7	IN / OUT	VCC_IO	Slave fifo data 7
J10	FX3_DQ8	IN / OUT	VCC_IO	Slave fifo data 8
J9	FX3_DQ9	IN / OUT	VCC_IO	Slave fifo data 9
K11	FX3_DQ10	IN / OUT	VCC_IO	Slave fifo data 10
L10	FX3_DQ11	IN / OUT	VCC_IO	Slave fifo data 11
K10	FX3_DQ12	IN / OUT	VCC_IO	Slave fifo data 12
K9	FX3_DQ13	IN / OUT	VCC_IO	Slave fifo data 13
J8	FX3_DQ14	IN / OUT	VCC_IO	Slave fifo data 14
G8	FX3_DQ15	IN / OUT	VCC_IO	Slave fifo data 15
K2	FX3_DQ16	IN / OUT	VCC_IO	Slave fifo data 16 / FMC_LA09_N
J4	FX3_DQ17	IN / OUT	VCC_IO	Slave fifo data 17 / FMC_LA12_N
K1	FX3_DQ18	IN / OUT	VCC_IO	Slave fifo data 18 / FMC_LA09_P
J2	FX3_DQ19	IN / OUT	VCC_IO	Slave fifo data 19 / FMC_LA10_P
J3	FX3_DQ20	IN / OUT	VCC_IO	Slave fifo data 20 / FMC_LA12_P
J1	FX3_DQ21	IN / OUT	VCC_IO	Slave fifo data 21 / FMC_LA08_P
H2	FX3_DQ22	IN / OUT	VCC_IO	Slave fifo data 22 / FMC_LA08_N
H3	FX3_DQ23	IN / OUT	VCC_IO	Slave fifo data 23 / FMC_LA10_N
F4	FX3_DQ24	IN / OUT	VCC_IO	Slave fifo data 24 / FMC_LA06_P
G2	FX3_DQ25	IN / OUT	VCC_IO	Slave fifo data 25 / FMC_LA05_P
G3	FX3_DQ26	IN / OUT	VCC_IO	Slave fifo data 26 / FMC_LA05_N
F3	FX3_DQ27	IN / OUT	VCC_IO	Slave fifo data 27 / FMC_LA06_N
F5	FX3_DQ28	IN / OUT	VCC_IO	Slave fifo data 28 / FMC_LA03_P / FTDI_CTS#
E1	FX3_DQ29	IN / OUT	VCC_IO	Slave fifo data 29 / FMC_LA03_N / FTDI_RTS#
E5	FX3_DQ30	IN / OUT	VCC_IO	Slave fifo data 30 / FMC_LA01_CC_N / FTDI_RXD

E4	FX3_DQ31	IN / OUT	VCC_IO	Slave fifo data 31 / FMC_LA01_CC_P / FTDI_TXD
F2	FX3_USB_EN	IN	VCC_IO	USB 3.0 device port enabled

Table 26: Cypress FX3 USB 3.0 controller pinout

2.10.10 USB 2.0 UART Device

The USB 2.0 UART device controller (U401) is connected to J400 (USB 2.0 Micro-B connector). It allows exchanging debug and control commands between the host computer and the FPGA module or FX3.

By default U401 is connected to both, the Mars module connector (Pins 34 and 36) and the FX3 controller (FX3_DQ28..31). Please make sure to drive the signals only from one device.

For more information about the USB 2.0 UART device please refer to the FT232RQ datasheet.

Pin	Signal	Direction	Description
22	CBUS0	OUT	RX LED (D401, Yellow)
21	CBUS1	OUT	TX LED (D402, Yellow)
10	CBUS2		Not connected
11	CBUS3		Not connected
9	CBUS4		Not connected
30	FTDI_TXD	OUT	RS232 TXD
2	FTDI_RXD	IN	RS232 RXD
8	FTDI_CTS#	IN	RS232 CTS#
32	FTDI_RTS#	OUT	RS232 RTS#

Table 27: USB 2.0 UART device pin assignment

3 Technical Data

3.1 Absolute Maximum Ratings

Symbol		Rating	Unit
VCC_12V_IN	Supply voltage relative to GND	-0.5 to 13.7	V
VCC_IO	I/O input voltage relative to GND	See Mars module user manual	
Temperature	Temperature range for wide range modules (W) Temperature range for commercial modules (C)	-25 to +85 0 to +65	°C

3.2 Recommended Operating Conditions

Symbol		Rating	Unit
VCC_12V_IN	Supply voltage relative to GND[1]	8 to 12 ±5%	V
V_IO	I/O input voltage relative to GND	See Mars module user manual	
Temperature	Temperature range for wide range modules (W) Temperature range for commercial modules (C)	-25 to +85 0 to +65	°C

Table 28: Recommended Operating Conditions

Note 1: The board may be operated down to 5V with reduced power handling capability. All 12V connections (fan, FMC, I/O connector) will then be out of specification.

Warning

The components used on the hardware are specified for the according temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

Warning

Please note that the input voltage (VCC_MAIN) must continuously rise at startup and continuously fall when switched off. A bouncing caused by switches or connectors can lead to peaks on the 5V supply that can damage the Mars PM3 as well as the inserted Mars module!

3.3 Mechanical data

Symbol	Value
Size	100.0 x 72.0 mm (Pico ITX)
Component height top	16 mm
Component height bottom	4.5 mm (Battery holder)
Weight	56 g (without Mars module)

Table 29: Mechanical data

4 Errata

4.1 Revision 02

The boards of revision R02 are marked as MA-PM3-B on the bottom side, close to the PCB edge.

4.1.1 FPGA Startup

The FPGA on the module cannot load the bitstream from the flash until the Cypress FX3 USB 3.0 controller has loaded its own application code from the flash or USB and releases the FPGA_INIT# line. This is due to the fact that with the current Cypress FX3 silicon the FX3 bootloader is actively driving some I/Os (e.g. the one FPGA_INIT# is connected) when the bootloader is running.

4.2 Revision 01

The boards of revision R01 are marked as MA-PM3-A on the bottom side, close to the PCB edge.

4.2.1 User EEPROM

The user EEPROM U902 is not assembled because it has its SDA and SCL connections interchanged.

4.2.2 USB 2.0 UART Device

The TXD and RXD lines are interchanged towards the FX3. Therefore the UART connection between FX3 (U301) and USB 2.0 UART device (U401) is not working.

4.2.3 I^2C Bus

I^2C bus is blocked due to D1003, D1000 and VCC_HDMI until FPGA is configured successfully (FPGA_DONE goes high).

4.2.4 USB_VBUS Sensing

The multiplexer U500 to select VBUS_A or VBUS_B for USB_VBUS is not placed to avoid unwanted current through the body diode of U500 if the board is not powered through the DC input connector. Therefore the USB bus voltage cannot be sensed by the FPGA module.

4.2.5 FPGA Configuration

The bitstream cannot be loaded into the FPGA by the FX3 (U301) due to missing connection from the FX3 to the FPGA_PROG# signal.

4.2.6 USB Connector Selection

The USB signals from the FPGA module cannot be routed to the USB device connector using S1200-3, since the select signal USB_SEL for the multiplexer U501 is 5V instead of 3.3V.

4.2.7 PCIe Interface

If the FPGA is not configured (FPGA_DONE low) then PCIE_PERST# is pulled down through D1000 and VCC_HDMI and may reset the host computer.

4.2.8 Ethernet LEDs

The LEDs on the Ethernet connector J700 only show activity on ETH0 correctly.

4.2.9 FPGA Startup

The FPGA on the module cannot load the bitstream from the flash until the Cypress FX3 USB 3.0 controller has loaded its own application code from the flash or USB and releases the FPGA_INIT# line.

4.2.10 FX3 Reset

The FX3 reset signal FX3_RESET_EXT# is connected to J801-2

5 Ordering and support

5.1 Ordering

Please use Enclustra's online request/order form for ordering or requesting information:

http://www.enclustra.com/en/orderenquire/

5.2 Support

Please follow the instructions on Enclustra's online support site:

http://www.enclustra.com/en/support/

Figures

Tables

Appendix A

5.3 Differential Pairs Net Length

Table 30 lists the length of the differential pairs on the Mars PM3 Board.

Differential Pair name	Net Length (mm)	Differential pair name	Net Length
PCIE_PER0_N	36.9	PCIE_PER0_P	38.6
PCIE_PER1_N	38.9	PCIE_PER1_P	37.5
PCIE_PET0_N	62.7	PCIE_PET0_P	59.4
PCIE_PET1_N	55.1	PCIE_PET1_P	56.9
PCIE_REFCLK_N	45.7	PCIE_REFCLK_P	45.4
FMC_CLK0_M2C_N	88.8	FMC_CLK0_M2C_P	89.4
FMC_CLK1_M2C_N	50.0	FMC_CLK1_M2C_P	51.2
FMC_LA00_CC_N	87.3	FMC_LA00_CC_P	86.4
FMC_LA01_CC_N	75.9	FMC_LA01_CC_P	77.2
FMC_LA02_N	74.8	FMC_LA02_P	77.0
FMC_LA03_N	64.4	FMC_LA03_P	65.3
FMC_LA04_N	77.7	FMC_LA04_P	78.8
FMC_LA05_N	56.7	FMC_LA05_P	56.7
FMC_LA06_N	68.9	FMC_LA06_P	69.4
FMC_LA07_N	68.7	FMC_LA07_P	67.9
FMC_LA08_N	71.9	FMC_LA08_P	72.1
FMC_LA09_N	60.6	FMC_LA09_P	60.0
FMC_LA10_N	69.3	FMC_LA10_P	69.7
FMC_LA11_N	67.0	FMC_LA11_P	68.3
FMC_LA12_N	63.2	FMC_LA12_P	62.7
FMC_LA13_N	60.7	FMC_LA13_P	62.6
FMC_LA14_N	62.5	FMC_LA14_P	61.9
FMC_LA15_N	58.7	FMC_LA15_P	58.8
FMC_LA16_N	62.6	FMC_LA16_P	62.5

FMC_LA17_CC_N	40.2	FMC_LA17_CC_P	40.3
FMC_LA18_CC_N	39.1	FMC_LA18_CC_P	39.8
FMC_LA19_N	47.4	FMC_LA19_P	46.2
FMC_LA20_N	45.1	FMC_LA20_P	44.4
FMC_LA21_N	53.3	FMC_LA21_P	52.0
FMC_LA22_N	43.5	FMC_LA22_P	42.7
FMC_LA23_N	43.0	FMC_LA23_P	43.1
FMC_LA24_N	63.0	FMC_LA24_P	60.9
FMC_LA25_N	43.3	FMC_LA25_P	42.8
FMC_LA26_N	58.1	FMC_LA26_P	56.3
FMC_LA27_N	40.4	FMC_LA27_P	39.9
FMC_LA28_N	62.3	FMC_LA28_P	60.1
FMC_LA29_N	69.6	FMC_LA29_P	68.5
FMC_LA30_N	68.6	FMC_LA30_P	67.3
FMC_LA31_N	36.5	FMC_LA31_P	33.9
FMC_LA32_N	35.9	FMC_LA32_P	35.4
FMC_LA33_N	39.7	FMC_LA33_P	39.1

Table 30: Differential pairs net length

References

[1] Enclustra Download Page
http://download.enclustra.com/#Mars_PM3

[2] *Enclustra General Business Conditions*
http://www.enclustra.com/en/products/gbc/

[3] Mars PM3 schematic: Available upon request

[4] Semtech SX150x datasheet: www.semtech.com

[5] 24AA128 EEPROM datasheet: www.microchip.com

[6] LM96080 datasheet: www.national.com

[7] CYUSB3014 datasheet: www.cypress.com