Pin Type	Pin Name	Direction seen from Module	Voltage Level	Description	Comments
All pins					- Applying a negative voltage or a voltage higher than the specified maximum, even for a short period of time, may damage the module permanently. The module does not have any protection against these hazards. - The ESD protection level available on each module pin is module- and pin-specific.
BOOT_MODE[3..0]	BOOT_MODE[3..0]	IN	V_IO_CFG	Boot-mode selection	- This pin selects between different module-specific boot modes. - The module contains pull-up or pull-down resistors on these pins for default setting. - For selecting the boot mode from the base board plaese refer to the user manual.
CFG_DONE	PS_DONE	OUT	V_IO_CFG	Configuration done signal	- The CFG_DONE pin is an output and indicates whether the SoC device has been configured successfully. - This pin may be left floating. - Enclustra recommends using a transistor or logic buffer to drive a status LED. Use a 10 kOhm to 47 kOhm pull-down to prevent this signal from floating when no module is installed. The source impedance of this pin is between 330 and 1000 Ohm. - Do not drive onto this pin on the base board.
ETH0_[A,B,C,D]_P/N ETH1_[A,B,C,D]_P/N	ETH0_[A,B,C,D]_P/N ETH1_[A,B,C,D]_P/N	BIDIR	Ethernet standard	Gigabit Ethernet pairs A-D	- These pins may be left floating if the Ethernet interface(s) is/are not used. - These pins should be connected to the A-D pin pairs of the RJ45 connector via suitable Gigabit Ethernet magnetics.
ETH[1,0]_LED[1,0]#	ETH[1,0]_LED[1,0]#	OUT	3.3 V	Ethernet LED, active-low	- These LEDs indicate link activity and status of the Ethernet interfaces (the exact function is module-specific). - Enclustra recommends connecting ETH[0,1]_LED0# signal to a yellow LED and ETH[0,1]_LED1# to a green LED on the RJ45 connector with a 150 Ohm series resistor to 3.3 V. - Do not add pull-up or pull-down resistors on this pin. Do not drive onto this pin. - This pin may be left floating if not used.
G	G	Ground			- On the base board, connect these pins to a ground plane with wide and very short traces.
GPIO0 GPIO1 GPIO2 GPIO3	PS_MIO34_DP_DO PS_MIO35_DP_HPD PS_MIO36_DP_DOE PS_MIO37_DP_DI	BIDIR	V_IO_CFG	User GPIO pins, module-specific	- Refer to the module's user manual for more information about the usage of these pins.
GPIO[7..4]_SD_D[7..4]	PS_MIO[42..39]_SD_D[7..4]	Module-specific	V_IO_CFG	Dual-function pins	- Refer to the module's user manual for more information about the usage of the dual-function pins.
GPIO8_SD_CD# GPIO9_SD_WP	PS_MIO45_SD_CD# PS_MIO44_SD_WP	Module-specific	V_IO_CFG	Dual-function pins	- Refer to the module's user manual for more information about the usage of the dual-function pins.
I2C_[0/1]_SCL I2C_[0/1]_SDA I2C_[0/1]_INT#	I2C_[MGMT/USER]_SCL I2C_[MGMT/USER]_SDA I2C_[MGMT/USER]_INT#	BIDIR/OD BIDIR/OD BIDIR/OD	3.3 V	I2C bus, clock I2C bus, data I2C bus, interrupt, active-low	- All signals are open drain. The modules already contain pull-ups on these pins. - When adding additional peripherals to this bus, make sure that there is no address conflict. - Do not drive these pins to a logic high level. Only allow these signals to be driven low. - 100 Ohm series resistors should be added between the module and I2C device on the base board when the I2C traces are long.
IO_<CLOC>_D[13..0]_P/N	IO_Bxx_L[24..1]_P/N	BIDIR	V_IO_Bxx	FPGA/SoC I/O pair number L[24..1] of bank Bxx, LVDS I/O pair	- The voltage on these pins may never exceed the voltage on the corresponding bank supply voltage. Check the FPGA/SoC datasheet for details.
IO_<CLOC>_D[13..0]_P/N	IO_Bxx_DS[3..0]	BIDIR	V_IO_Bxx	FPGA/SoC I/O, single-ended I/O	- The voltage on these pins may never exceed the voltage on the corresponding bank supply voltage. Check the FPGA/SoC datasheet for details.
IO_<CLOC>_D[13..0]_BC_P/N	IO_Bxx_L[24..1]_BC_P/N	BIDIR	V_IO_Bxx	FPGA/SoC I/O pair number L[24..1] of bank Bxx, LVDS I/O pair, connected to byte-lane clock input (BC)	- The voltage on these pins may never exceed the voltage on the corresponding bank supply voltage. Check the FPGA/SoC datasheet for details. - Refer to the module's schematics/user manual and to the FPGA/SoC datasheet for more information about the connection to the FPGA/SoC clocking resources.

IO_<CLOC>_D[13..0]_GC_P/N	IO_Bxx_L[24..1]_GC_P/N	BIDIR	V_IO_Bxx	FPGA/SoC I/O pair number L[24..1] of bank Bxx, connected to global clock input (GC)	- The voltage on these pins may never exceed the voltage on the corresponding bank supply voltage. Check the FPGA/SoC datasheet for details. - Refer to the module's schematics/user manual and to the FPGA/SoC datasheet for more information about the connection to the FPGA/SoC clocking resources.
JTAG_TDI JTAG_TDO JTAG_TCK JTAG_TMS	JTAG_TDI JTAG_TDO JTAG_TCK JTAG_TMS	IN OUT IN IN	V_IO_CFG	JTAG chain, test data input JTAG chain, test data output JTAG chain, test clock JTAG chain, test mode select	- Enclustra recommends adding a 22 Ohm series termination resistor on the TCK signal and 100 Ohm series termination resistor on the other signals between the module and the JTAG header. - Enclustra recommends adding low-capacitance (<5 pF) ESD protection diodes on the connector side of the series resistors close to the JTAG header. - These pins have pull-ups / pull-downs as required by the FPGA/SoC on the module. Do not add additional pull-up / pull-down resistors. - These pins may be left floating.
MGT_<CLOC>_CLK[1..0]_P/N	MGT_Bxx_CLK[1..0]_P/N	IN		Multi-gigabit-transceiver reference clocks for bank Bxx	- Use AC coupling capacitors for connection to oscillator or to receiving device. The module does not contain any AC coupling capacitors on those signals. - Check the FPGA/SoC vendors datasheet on specific requirements if unused.
MGT_<CLOC>_RX[3..0]_P/N	MGT_Bxx_RX[3..0]_P/N	IN		Multi-gigabit-transceiver receive differential pair [3..0] of bank Bxx	- Use AC coupling capacitors for the connection to the transceiver. The module does not contain any AC coupling capacitors on those signals. - Check the FPGA/SoC vendors datasheet on specific requirements if unused.
MGT_<CLOC>_TX[3..0]_P/N	MGT_Bxx_TX[3..0]_P/N	OUT		Multi-gigabit-transceiver transmit differential pair [3..0] of bank Bxx	- Transmitter should be AC coupled to the receiver. The module does not contain any AC coupling capacitors on those signals. - Check the FPGA/SoC vendors datasheet on specific requirements if unused.
PERST0#	PS_MIO33_PERSTPS#_LED0#	BIDIR	V_IO_CFG	Dual-function pin, PCIe reset signal 0, LED0	- When used as PERST# signal, it can be input (for PCIe endpoint applications) or output (for root-complex applications) or it can be used as GPIO. - This pin may be left floating.
PERST1#	PS_MIO32_PERSTPL#_LED1#	BIDIR	V_IO_CFG	Dual-function pin, PCIe reset signal 1, LED1	- When used as PERST# signal, it can be input (for PCIe endpoint applications) or output (for root-complex applications) or it can be used as GPIO. - This pin may be left floating.
PWR_EN	PWR_EN	IN, OD	3.3 V	Power enable, active-high	- Do not drive this pin to a logic high level. Only allow this signal to be driven low. - The module contains a pull-up on this signal. A pull-up on the base board is not needed. - This pin should be driven low on the base board when the VIN_MOD power input is below the specified voltage range. Usually, the power good signal of the VIN_MOD source should be connected to this pin.
PWR_GOOD	PWR_GOOD	OUT, OD	3.3 V	Power good, active-high	- The module contains a pull-up on this signal. A pull-up on the base board is not needed. - Some of the module's power converters pull this pin low when their output voltage is below a power good threshold. - Do not power the V_IO pins when PWR_GOOD is not active. Enclustra recommends using a load switch, which uses PWR_GOOD as enable signal.
RST_CPU#	PS_SRST#	IN, OD	V_IO_CFG	Soft-reset	- The signal is used as a soft-reset input. - Do not drive this pin to a logic high level. Only allow this signal to be driven low. - The module contains a pull-up on this signal. - Make sure that components connected to this pin on the base board are V_IO_CFG-tolerant. - Enclustra recommends connecting this signal to the JTAG connector for SoC processor debugging.

RST_SYS#	PS_POR#	IN, OD	V_IO_CFG	Power-on-reset	- The signal is used as a power-on-reset input. - This pin should be driven low after power-on until some FPGA/SoC-specific time after all V_IO* and V_IO_CFG power inputs are stable. Either a voltage supervisor device or a buffered PWR_GOOD signal from these respective power converters on the base board should be connected to this pin using an open drain circuit. - A minimum delay of 10 ms from the assertion of PWR_GOOD to the release of the RST_SYS# signal is required. - Enclustra recommends adding a push-button to ground on this pin. - Do not drive this pin to a logic high level. Only allow this signal to be driven low. - The module contains a pull-up on this signal. - Make sure that components connected to this pin on the base board are V_IO_CFG-tolerant.
RSVD_<CLOC>	DNU or Module-specific			Do not use	- Do not use this pin. Leave these pins floating. - Refer to the module's user manual for more information about the usage of these pins.
NC	NC			Not connected	- This pin is not connected on this module. - For base boards that are designed to be compatible with more than one module, use this pin according to the module that doesn't have NC on it.
SD_D[3..0] SD_CLK SD_CMD	SD_D[3..0] SD_CLK SD_CMD	BIDIR OUT BIDIR	V_IO_CFG	SD data input/output SD clock output SD command input/output	- Please note that external pull-ups are needed for SD card operation. - Refer to the module's user manual for more information about the usage of these pins.
UART0_RX, UART1_RX	UART0_RX, UART1_RX	IN	V_IO_CFG	UART RX	- UART RX is an MPSoC input.
UART0_TX, UART1_TX	UART0_TX, UART1_TX	OUT	V_IO_CFG	UART TX	- UART TX is an MPSoC output.
USB0_CPEN USB1_CPEN	USB0_CPEN USB1_CPEN	OUT	3.3 V	USB VBUS enable output, active-high	- In USB 2.0 host and USB 2.0 OTG mode, Enclustra recommends to use a USB-type active-high load switch on the base board between a 5 V power supply and USB_VBUS. Add >= 120 uF (host) or 10 uF (OTG) of capacitance on the USB connector-side of the load switch as per the USB standard. - This pin may be left floating.
USB0_D_P/N USB1_D_P/N	USB0_D_P/N USB1_D_P/N	BIDIR	USB standard	USB high speed data lines	- The USB data lines connect to a module-specific USB interface, if available. - The USB data lines may be left floating if the USB interface is not used. - Enclustra recommends adding low-capacitance (<= 1 pF) ESD protection diodes close to the USB connector.
USB0_ID USB1_ID	USB0_ID USB1_ID	IN	USB standard	USB OTG ID input	- In USB 2.0 OTG mode, the USB_ID pin is used to detect if a host or a device has been connected. Connect it to the AB-type USB connector. - In USB 2.0 or USB 3.0 device mode, this pin should be left floating. The ID pin of the USB connector (if any) should be left floating. - In USB 2.0 host mode, this pin should be connected to GND. The ID pin of the USB connector (if any) should be connected to GND. - This pin may be left floating.
V_BAT	V_BAT	IN	Module-specific	Battery power input	- This pin connects to the VBAT of the SoC. - Use a Schottky diode and a 10 kOhm series resistor between the battery on the base board and this pin. - The diode is required because some modules may source power to this pin from a rechargeable battery. - When not using a battery on the base board, refer to the FPGA/SoC device datasheet on how to connect this pin. Xilinx MPSoC requires GND or VCC_PSAUX when not using (see DS925 p. 5, footnote7).

V_IO_<CLOC>	V_IO_Bxx	IN	Module-specific	Supply pin for I/O bank Bxx, mapped to the corresponding I/O group	- These pins needs to be connected to an adequate power supply on the base board. - Enclustra recommends adding a 0.1 uF to 1 uF (10 V) capacitor on the base board per pin connected with short and wide traces. - Please check the voltage range supported by the connected FPGA/SoC. Some banks may only have a restricted voltage range. - Do not drive the V_IO_Bxx pins when PWR_GOOD is not active.
V_IO_CFG	V_IO_CFG	IN	Module-specific	Supply for configuration bank of FPGA/SoC	- These pins needs to be connected to an adequate power supply on the base board. - Enclustra recommends adding a 0.1 uF to 1 uF (10 V) capacitor on the base board per pin connected with short and wide traces. - Please check the voltage range supported by the connected FPGA/SoC. Some banks may only have a restricted voltage range. - Do not power the V_IO_CFG pins when PWR_GOOD signal is not active.
V_MOD0	V_MOD_PS	IN		12 V module main supply pins	- This pin needs to be connected to an adequate power supply on the base board. - Enclustra recommends adding at least a 4.7 uF to 10 uF (25 V) capacitor on the base baord per pin connected with short and wide traces. - Enclustra recommends a maximum voltage ripple of +-5% of the average value on this pin. - Enclustra recommends adding reverse and over-voltage protection circuitry on the base board.
V_MOD1	V_MOD_PL_W V_MOD_PL_X	IN		12 V module main supply pins	- This pin needs to be connected to an adequate power supply on the base board. - Enclustra recommends at least 4.7 uF to 10 uF (25 V) capacitor on the base board per pin connected with short and wide traces. - Enclustra recommends a maximum voltage ripple of +-5% of the average value on this pin. - V_MOD0 and V_MOD1 may be connected together on the base board. - Enclustra recommends adding reverse and over-voltage protection circuitry on the base board.
V_USB0 V_USB1	V_USB0 V_USB1	IN	5 V	USB VBUS detect input	- The USB_VBUS is used to detect USB power. - The module does not draw power from this pin. - This pin may be left floating if the USB interface is not used.

Notes:

#=active-low signal
CLOC=connector location
IN=Input
OUT=Output
BIDIR=Bidirectional
OD=open drain

Disclaimers

All pinout and pin information is provided as-is without assurance of correctness or completeness.
All information is subject to change at any time without notice.
Please verify all data with Enclustra's user manuals, FPGA/SoC and other components vendor's documentation.
Enclustra recommends checking the module's and the FPGA/SoC and other components errata sheets.

Version: 04 July 2023